MAIL STOP PETITION
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Pun Jae CHOI et al.
Application No.:	10/593,088
Int'l App. No.:	PCT/KR2005/000036
Filing Date:	September 15, 2006
Title:	ANTI-REFLECTED HIGH EFFICIENCY LIGHT EMITTING DIODE DEVICE
Attorney Docket:	8947-000222/US

Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

November 10, 2008

PETITION UNDER 37 CFR § 1.42 - 1.47 FOR ACCEPTANCE OF AN APPLICATION MISSING INVENTOR(S)

Sir:

Pursuant to 37 C.F.R. § 1.47(a), Applicants petition to proceed with the prosecution of the above-identified application, which names Pun Jae CHOI, Jin Soo PARK, Seong Han KIM, Myeong Kook GONG and Hyeon Ryong CHOI, in the name of Myeong Kook GONG.

The basis for this Petition is that four of the named inventors, specifically Pun Jae CHOI, Jin Soo PARK, Seong Han KIM, and Hyeon Ryong CHOI, are unavailable to sign the declaration and power of attorney in this application. In connection with this Petition, Applicants concurrently submit the Declaration of Dr. Se Jun OH (Exhibit 1) detailing the factual circumstances surrounding unavailability of these four inventors to complete the Declaration for this application.

The Declaration submitted herewith details the efforts by the inventors' representatives, Dr Se-Jun OH to secure the signatures of these four inventors Jae CHOI, Jin Soo PARK, Seong Han KIM, and Hyeon Ryong CHOI and includes

documentary evidence (Declaration Attachments 1-8) regarding the efforts to obtain the signatures of the inventors.

For the convenience of the Office, Applicants submit herewith a copy of the executed Declaration (executed only by the fourth inventor, Myeong-Kook GONG). This Declaration was originally submitted on September 9, 2008, together with a Response to Notice of Missing Requirements

Applicants submit a check in the amount of $130.00 for the Petition fee, and a check for $1,300.00 to pay for the fourth and fifth-month extension of time for responding to the Notice of Missing Requirements, a three-month extension of time having previously been paid on September 9, 2008.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By _____

John A. Castellano, Reg. No. 35,094

JAC/pw

P.O. Box 8910
Reston, Virginia 20195
(703) 668-8000

Enclosures: Declaration in Support of Petition (with attachments)
Copy of Declaration (executed by only 1 inventor)
Response to Notification of Defective Response
Check for $130
Check for $1,300

11/12/2008 GFREY1 00000015 10593088

01 FC:1464 130.00 OP
02 FC:1255 2350.00 OP

Atty. Dkt. No.:8947-000222/US

DECLARATION AND POWER OF ATTORNEY (POA)

As a below named inventor, I hereby declare that:

My residence, mailing address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

ANTI-REFLECTED HIGH EFFICIENCY LIGHT EMITTING DIODE DEVICE

the specification of which (check one)

- ☐ is attached hereto.
  or
- ☒ was filed on January 7, 2005 as Application Serial No. or PCT International Application No. PCT/KR2005/000036 and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. §§ 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or any PCT international application having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)				
APPN. SERIAL NO.	COUNTRY	DATE FILED (MM/DD/YYYY)	PRIORITY CLAIM	
			Yes	No
10-2004-0018139	KOREA	March 17, 2004	☒	☐
			☐	☐
			☐	☐

Atty. Dkt. No.: 8947-000222/US

DEC. AND POA Cont'd

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

PRIOR PROVISIONAL APPLICATION(S)	
APPN. SERIAL NO.	DATE FILED (MM/DD/YYYY)

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) listed below:

PRIOR U.S. APPLICATION(S)		
APPN. SERIAL NO.	DATE FILED (MM/DD/YYYY)	STATUS - PATENTED, PENDING, ABANDONED

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY

I hereby appoint the following attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

Thomas S. Auchterlonie	Reg. No. 37,275
John A. Castellano	Reg. No. 35,094
Terry L. Clark	Reg. No. 32,644
Donald J. Daley	Reg. No. 34,313
Gary D. Yacura	Reg. No. 35,416

and all individuals assigned to Customer No. **30593**.

Atty. Dkt. No.: 8947-000222/US

DEC. AND POA Cont'd

CORRESPONDENCE ADDRESS

I request the Patent and Trademark Office to direct all correspondence and telephone calls relative to this application to Harness, Dickey & Pierce, P.L.C., Customer No. 30593, P.O. Box 8910, Reston, Virginia, 20195, (703) 668-8000.

Full name of sole or first inventor: Pun-Jae CHOI

Inventor's signature: _____

Date: _____

Residence: 203-1101 Hansol Apt., Songgang-dong, Yuseong-gu, Daejeon KOREA

Citizenship: Republic of Korea

Mailing Address: Same as above

Full name of second joint inventor: Jin-Soo PARK

Inventor's signature: _____

Date: _____

Residence: 629 Beonji, Deongnim-ri, Jusan-myeon, Buan-gun, Jeollabuk-do, KOREA

Citizenship: Republic of Korea

Mailing Address: Same as above

Full name of third joint inventor: Seong-Han KIM

Inventor's signature: _____

Date: _____

Residence: 204-303 Hansol Apt., Songgang-dong, Yuseong-gu, Daejeon, KOREA

Citizenship: Republic of Korea

Mailing Address: Same as above

Atty. Dkt. No.: 8947-000222/US

DEC. AND POA Cont'd

Full name of fourth joint inventor: Myeong-Kook GONG

Inventor's signature: _____

Date: 2008. 6. 25.

Residence: 901-2003 LG-XI Apt., 869 Beonji, Sanghyeon-dong, Yongin, Gyeonggi-do KOREA

Citizenship: Republic of Korea

Mailing Address: Same as above

Full name of fifth joint inventor: Hyeon-Ryong CHO

Inventor's signature: _____

Date: _____

Residence: 523-908 5 Danji Jugong Apt., Maetan 1-dong, Paldal-gu, Suwon, Gyeonggi-do KOREA

Citizenship: Republic of Korea

Mailing Address: Same as above

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Attorney Docket:	8947-000222/US

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314
Mail Stop AMENDMENT

DECLARATION IN SUPPORT OF PETITION UNDER 37 CFR 1.47

I, Se-Jun OH, declare:

Proof of pertinent facts showing the first inventor is unavailable:

(1) I mailed a cover letter and a copy of the patent application as filed along with a declaration and assignment to Pun Jae CHOI to his last known address at 203-1101 Hansol Apt., Songgang-dong, Yuseong-gu, Daejeon, 305-758, Republic of Korea, on June 16, 2008 by certified-content mail;

(2) The mail receipt shows that the copy was sent to Pun Jae CHOI. See Attachment 1 and its English translation.

(3) The package to Pun Jae CHOI was returned with an indication that the recipient is not resident at the address (no particular reason). See Attachment 2 and its English translation.

(4) I again mailed a cover letter and a copy of the patent application as filed along with a declaration and assignment to Pun Jae CHOI to his last known address at 203-1101 Hansol Apt., Songgang-dong, Yuseong-gu, Daejeon, 305-758, Republic of Korea, on August 20, 2008 by certified-content mail;

(5) The mail receipt shows that the copy was sent to Pun Jae CHOI. See Attachment 3 and its English translation.

(6) The package to Pun Jae CHOI was returned with an indication that the recipient is not resident at the address (not resident). See Attachment 4 and its English translation.

Proof of pertinent facts showing the second inventor is unavailable:

(7) I mailed a cover letter and a copy of the patent application as filed along with a declaration and assignment to Jin-Soo PARK to his last known address at 629 Beonji, Deongnim-ri, Jusan-myeon, Buan-gun, Beollabuk-do, Republic of Korea, on June 16, 2008 by certified-content mail;

(8) The mail receipt shows that the copy was sent to Jin-Soo PARK. See Attachment 1 and its English translation.

(9) I have not received any response from Jin-Soo PARK;

(10) I again mailed a cover letter and a copy of the patent application as filed along with a declaration and assignment to Pun Jae CHOI to his last known address at 203-1101 Hansol Apt., Songgang-dong, Yuseong-gu, Daejeon, 305-758, Republic of Korea, on August 20, 2008 by certified-content mail;

(11) The mail receipt shows that the copy was sent to Pun Jae CHOI. See Attachment 3 and its English translation.

(12) Again I have not received a response from Jin-Soo PARK.

Proof of pertinent facts showing the third inventor is unavailable:

(13) I mailed a cover letter and a copy of the patent application as filed along with a declaration and assignment to Seong Han KIM to his last known address at 204-303 Hansol Apt., Songgang-dong, Yuseong-gu, Daejeon, 305-758, Republic of Korea, on June 16, 2008 by certified-content mail;

(14) The mail receipt shows that the copy was sent to Seong Han KIM. See Attachment 1 and its English translation.

(15) The package mailed to Seong Han KIM was returned with an indication that the recipient is not resident at the address. See

Attachment 5 and its English translation.

Proof of pertinent facts showing the fifth inventor is unavailable:

(16) I mailed a cover letter and a copy of the patent application as filed along with a declaration and assignment to Hyeon-Ryong CHO to his last known address at 523-908 5 Danji Jugong Apt., Maetan 1-dong, Paldal-gu, Suwon, Gyeonggi-do, 443-709, Republic of Korea, on June 16, 2008 by certified-content mail;

(17) The mail receipt shows that the copy was sent to Hyeon-Ryong CHO. See Attachment 1 and its English translation.

(18) The package mailed to Hyeon-Ryong CHO was returned with an indication that the recipient is not resident at the address (house moved). See Attachment 6 and its English translation.

(19) A copy of the cover letter and package mailed on June 19, 2008 is attached as Attachment 7.

(20) A copy of the cover letter and package mailed on August 20, 2008 is attached as Attachment 8.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine and imprisonment, or both, under Title 18, United States Code, § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Date: NOV 6, 2008

Dr. Se-Jun OH, Ph.D
Patent Attorney

Attachment 1

Post Office
www.epost.go.kr

No. 11257397

Yeoksam-1-Dong Post Office, Seoul
1st Floor, Korean Centre of Intellectual Property,
131 Teheranro, Gangnam-gu, Seoul.
Tel) (02)552-0159
Business Reg. No.: 101-83-02925

Receptionist: Desk No. 12, Han, Sang-Hwe
Application date: 2008-06-19 13:50
Total Cost: 36,550 won (Immediate payment of 36,550 won, cash: 36,550 won, Credit Card: 0 won)
VAT imposed Value of Supply: 0 won
VAT: 0 won

<Domestic Registered Delivery>
Sender: Se-Jun OH
Koryo International Patent & Law Office, Gangnam-gu, Seoul 135-080
Number of Letters: 5
Cost: 36,550 won (Paid Amount: 36,550 won, Stamps Pasted: 0 won)

Reg. No.	Cost	Recipients
3110512004660 Next-Day Special Delivery	22,910	305758 Choi, Pun-Jae
3110512004661 Next-Day Special Delivery	3,410	579922 Park, Jin-Soo
3110512004662 Next-Day Special Delivery	3,410	305758 Kim, Seong Han
3110512004663 Next-Day Special Delivery	3,410	448529 Gong, Myeong-Kook
3110512004664 Next-Day Special Delivery	3,410	443709 Cho, Hyeon-Ryong

---

우 체 국
<www.epost.go.kr>

No. : 11257397
서울역삼1동 우체국
서울시 강남구 테헤란로 131 한국지식재산센터빌딩 1층 (
전 화 : 02-552-0159
사업자No. : 101-83-02925
접 수 자 : 창구12 한상희
접수일자 : 2008-06-18 13:50
총 요 금 : 36,550원(즉납:36,550원)
(현 금 : 36,550원
신용카드 : 0원)
부가세과세 공급가액 : 0원
부 가 세 : 0원

<국내등기우편물>
발 송 인 : 135-080 고려국제특허 오세준 서울 강남구
통 수 : 5통
요 금 : 36,550원(수납요금:36,550원
우표첩부 : 0원)

등기번호	요금	수취인
3110512004660	22,910	305758 최번재
익일특급 등문내용		
3110512004661	3,410	579922 박진수
익일특급 등문내용		
3110512004662	3,410	305758 김성한
익일특급 등문내용		
3110512004663	3,410	448529 공명국
익일특급 등문내용		
3110512004664	3,410	443709 조현룡
익일특급 등문내용		

2007년도 고객만족도 9년 연속 1위 수상!
2007년도 택배부분 고객만족도 5년연속
1위 수상!

- 반송시에는 환부료를 받습니다.
- 이 영수증은 손해배상 등의 청구에 필요하오니 보관하십시오.
- 우편물 송달기준 적용곤란지역은 예정된 배달일보다 더 소요될 수 있습니다.
- 인터넷우체국(http://www.epost.go.kr)에서 등기우편물 배달조회가 가능합니다.
- 배달조회기간은 1년(내용증명 : 3년)입니다.
- 상담문의전화 : 1588-1300

Attachment 2

[Sender]

Attorney - Oh, Se-Jun

KORYO INTERNATIONAL PATENT & LAW OFFICE 3rd Fl, 827-25, Yeoksam-dong, Kangnam-ku, Seoul 135-080 Republic of Korea

Tel: 82-2-2186-8300

Fax: 82-2-2186-8301~2

Homepage: http://www.krpatent.co.kr

Representing Sender: Kim, Yeon-Jung

[Recipient]

Choi, Pun-jae

203-1101 Hansol Apt,

Songgang-dong, Yuseong-gu,

Daejeon,

305-758

[Collection and Delivery]

Han, Kook-hee

Tel: 042)828-8231

Number of delivery : (2)

NOTE: storage until 2008.06.25

[Next day special delivery]

2008.06.19

\2410

305-758

Daejeon Daejeonyuseong

31105-12004660 Seoul Yeoksam 1 dong

[Returned]

2008.08.21 Daejeonyuseong

	House-moved
	Recipient absent
	Unidentified address
	Refusal upon receiving
	Unidentified recipient
0	Shut doors absent

高麗國際特許法律事務所

변리사 오 세 준 　　　長

서울特別市 江南區 驛三洞 827-25 테라빌 3層
代表電話 : (02) 2186-8300
FAX : (02) 2186-8301/2
Homepage : http://www.krpatent.co.kr
135-080

담당 : 김 연 정

보관기간 6 월 25 일

집 배 담 당
T.042)828-8231
한 국 희
(2)회 배달
기타의견:

반 송
2008. 06. 20.
대전유성

특별 2008/06/19 ₩2410=
대전 대전유성 305-758
31105-12004660 서울역삼1동

본인 수취 불가 시
반드시 빠른 반송 부탁드립니다.

대전시유성구 송강동 한솔아파트 203동 1101호
최번재 귀하
우편번호: 305-758

Attachment 3

Post Office
www.epost.go.kr

No. 11383053

Yeoksam-1-Dong Post Office, Seoul
1st Floor, Korean Centre of Intellectual Property,
131 Teheranro, Gangnam-gu, Seoul.
Tel) (02)552-0159
Business Reg. No.: 101-83-02925

Receptionist: Desk No. 13, Hwang, Mun-suk
Application date: 2008-08-20 15:02
Total Cost: 26,320 won (Immediate payment of 26,320 won, cash: 26,320 won, Credit Card: 0 won)
VAT imposed Value of Supply: 0 won
VAT: 0 won

<Domestic Registered Delivery>
Sender: Kim, Yeon-Jung
Koryo International Patent & Law Office, Gangnam-gu, Seoul 135-080
Number of Letters: 2
Cost: 26,320 won (Paid Amount: 26,320 won, Stamps Pasted: 0 won)

Reg. No.	Cost	Recipients
3110513012244	22,910	305758 Choi, Pun-Jae
Next-Day Special Delivery		
3110513012245	3,410	579922 Park, Jin-Soo
Next-Day Special Delievery		

우 체 국
<www.epost.go.kr>

No. : 11383853

서울역삼1동 우체국
서울시 강남구 테헤란로 131 한국지식재산센터빌딩 1층 (역삼동 647-8번지)
전 화 : 02-552-8159
사업자No. : 101-83-82825
접 수 자 : 창구13 황문숙
접수일자 : 2008-08-20 15:02
총 요 금 : 26,320원(즉납:26,320원)
(현 금 : 26,320원
신용카드 : 0원)
부가세과세 공급가액 : 0원
부 가 세 : 0원

<국내등기우편물>
발 송 인 : 135-080 고려국제특허 김연정 서울 강남구
통 수 : 2통
요 금 : 26,320원(수납요금:26,320원
우표첩부 : 0원)

등기번호	요금	수취인
3118513812244	22,910	305758 최번재
익일특급 등문내용		
3118513812245	3,410	579922 박진수
익일특급 등문내용		

2007년도 고객만족도 9년 연속 1위 수상!
2007년도 택배부분 고객만족도 5년연속 1위 수상!

- 반송시에는 반송료를 받습니다.
- 이 영수증은 손해배상 등의 청구에 필요하오니 보관하십시오.
- 우편물 송달기준 적용곤란지역은 예정된 배달일보다 더 소요될 수 있습니다.
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- 배달조회기간은 1년(내용증명 : 3년)입니다.
- 상담문의전화 : 1588-1300

Attachment 4

[Sender]

Attorney - Oh, Se-Jun

KORYO INTERNATIONAL PATENT & LAW OFFICE 3rd Fl, 827-25, Yeoksam-dong, Kangnam-ku, Seoul 135-080 Republic of Korea

Tel: 82-2-2186-8300

Fax: 82-2-2186-8301~2

Homepage: http://www.krpatent.co.kr

Representing Sender: Kim, Yeon-Jung

[Recipient]

Choi, Pun-jae

203-1101 Hansol Apt,

Songgang-dong, Yuseong-gu,

Daejeon,

305-758

[Collection and Delivery]

Han, Kook-hee

Tel: 042)828-8231

Number of delivery : ( )

[Next day special delivery]

2008.08.20

\2410

305-758

Daejeon Daejeonyuseong

31105-13012244 Seoul Yeoksam 1 dong

[Returned]

2008.08.21 Daejeonyuseong

	House-moved
	Recipient absent
	Unidentified address
	Refusal upon receiving
0	Unidentified recipient
	Shut doors absent

Recipient is not resident in the supposed address!

高麗國際特許法律事務所

F 변리사 오 세 준

서울特別市 江南區 驛三洞 827-25 테라빌 3層
代表電話 : (02) 2186-8300
F A X : (02) 2186-8301/2
Homepage : http://www.krpatent.co.kr
135-080

발신메모: 강명자: 76 0278

수취인 미거주

접수 배달 담당
T.042)828-8231
관 리 희
(회 배달
기타의견:

본인 수취 불가 시
반드시 빠른 반송 부탁드립니다.

대전시유성구 송강동 한솔아파트 203동 1101호
최민재 귀하
우편번호: 305-758

[Sender]
Attorney - Oh, Se-Jun
KORYO INTERNATIONAL PATENT & LAW OFFICE 3rd Fl, 827-25, Yeoksam-dong, Kangnam-ku, Seoul 135-080 Republic of Korea
Tel: 82-2-2186-8300
Fax: 82-2-2186-8301~2
Homepage: http://www.krpatent.co.kr
Representing Sender: Kim, Yeon-Jung

[Recipient]
Kim, Seong-Han
204-303 Hansol Apt,
Songgang-dong, Yuseong-gu,
Daejeon,
305-758

[Collection and Delivery]
Han, Kook-hee
Tel: 042)828-8231
Number of delivery : ( )

[Next day special delivery]
2008.06.19
\2410
305-758
Daejeon Daejeonyuseong
31105-12004662 Seoul Yeoksam 1 dong

[Returned]
2008.06.20 Daejeonyuseong

	House-moved
	Recipient absent
	Unidentified address
	Refusal upon receiving
	Unidentified recipient
	Shut doors absent

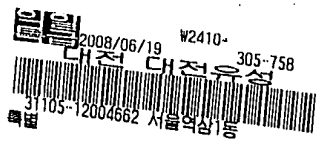
Recipient is not resident in the supposed address!

高麗國際特許法律事務所

변리사 오 세 준

서울特別市 江南區 驛三洞 827-25 테라빌 3層
代表電話 : (02) 2186-8300
F A X : (02) 2186-8301/2
Homepage : http://www.krpatent.co.kr
135-080

담당 : 76 0078



집 배 담 당
T.042)828-8231
한 국 희
( )회 배달
기타의견:

수취인 미거주!

본인 수취 불가 시
반드시 빠른 반송 부탁드립니다.

대전시 유성구 송강동 한솔아파트 204동 303호
김성한 귀하
우편번호: 305-758

[Sender]
Attorney - Oh, Se-Jun
KORYO INTERNATIONAL PATENT & LAW OFFICE 3rd Fl, 827-25, Yeoksam-dong, Kangnam-ku, Seoul 135-080 Republic of Korea
Tel: 82-2-2186-8300
Fax: 82-2-2186-8301~2
Homepage: http://www.krpatent.co.kr
Representing Sender: Kim, Yeon-Jung

[Recipient]
Cho, Hyeon-Ryong
523-908 5 danji Jugong Apt.
Maetan 1-dong, Paldal-gu, Suwon
Gyeonggi-do,
443-709

[Collection and Delivery]
Lee, Sun-Ju
Tel: 011-9272-3047

[Next day special delivery]
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31105-12004664 Seoul Yeoksam 1 dong

[Returned]
2008.06.20 Dongsuwon

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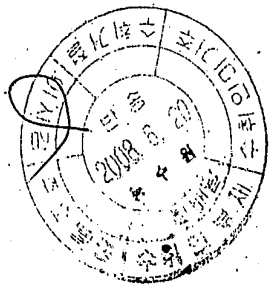
	Unidentified recipient
	Shut doors absent

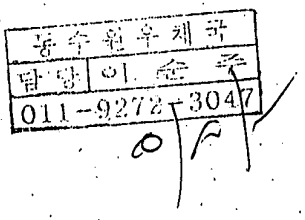
高麗國際特許法律事務所

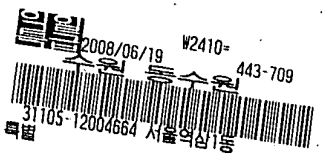
변리사 오 세 준

울特別市 江南區 驛三洞 827-25 테라빌 3層
表電話 : (02) 2186-8300
A X : (02) 2186-8301/2
omepage : http://www.krpatent.co.kr
35-080

앞앞: 76 면 76







본인 수취 불가 시
반드시 빠른 반송 부탁드립니다.

경기도 수원시 팔달구 매탄1동 주공아파트 5단지
523동 908호
조현룡 귀하
우편번호: 443-709

Attachment 7

KORYO INTERNATIONAL PATENT & LAW OFFICE

3rd Floor, 827-25 Yeoksam-dong, Gangnam-gu, Seoul

http://www.krparent.co.kr
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Tel: 02-2186-8300
FAX: 02-2186-8301/2

2008-06-19

Recipient: **Choi, Pun-Jae** 203-1101 Hansol Apt., Songgang-dong, Yuseong-gu, Daejeon (KR)
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Gong, Myeong-Kook 901-2003 LG-XI Apt., 869 Beonji, Sanghyeon-dong, Yongin, Gyeonggi-do (KR)
Cho, Hyeon-Ryong 523-908 5 Danji Jugong Apt., Maetan 1-dong, Paldal-gu, Suwon, Gyeonggi-do (KR)

Sender: Koryo patent & law office Yeon-jung Kim(Administration), Se-Jun Oh(Technical)

Subject: Request for signing Declaration/Assignment forms. (For late submission)

---

1. Patent Registration Status

Country	U.S.	Type of Application	PCT National Phase Entry
Office Reference No.	XP16327-US		
Korean Application No.	P2004-18139	Korean Application Date	Mar 17, 2004
PCT International Application No.	PCT/KR2005/000036	PCT International Application Date	Jan 07, 2005
Local Attorney	HDP	Date of Commission	Sep 15, 2006
Foreign Application No.	10/593,088		
Inventors	Choi, Pun-jae; Gong, Myung-kook; Park, Jin-soo; CHO, Hyeon Ryong; KIM, Seong Han		
Name of Invention	ANTI-REFLECTED HIGH EFFICIENCY LIGHT EMITTING DIODE DEVICE		

1. We note that the US national phase entry of above PCT/KR2005/000036 was completed on September 15, 2008. We enclose declaration and assignment forms for execution in order to complete formality of entering the US national phase. Please have the inventors sign and date in the documents, and return via Fax/E-mail before July 9, 2008.
2. Please refer to the enclosed Declaration/Assignment forms

3. If there are any inquiries, please contact the sender, Se-Jun Oh(technical) or Yeong-Jung Kim(administration) of Koryo Patent & Law Office.
(Tel. 02-2186-8300, E-Mail: kr@krpatent.co.kr)

Koryo International Patent & Law Office

※Enclosed: 1. Application as filed
2. Declaration/Assignment Forms.

I hereby confirm that the concerned mail has been posted as a certification-of-content mail on June 19, 2008.
No. 3110512004660-3110512004664

Post Master,
Yeoksam-1-Dong Post Office, Seoul

고려국제특허법률사무소

서울시 강남구 역삼동 827-25 테라빌 3층

http:// www. krpatent.co.kr
E-maill : kr@krpatent.co.kr
TEL: 02-2186-8300
FAX : 02-2186-8301/2

2008 년 6 월 19 일

수 신 : 최번재(대전시 유성구 송강동 한솔아파트 203 동 1101 호
박진수(전라북도 부안군 주산면 덕림리 629 번지
김성한(대전시 유성구 송강동 한솔아파트 204 동 303 호
공명국(경기도 용인시 상현동 869 번지 LG-XI 아파트 901 동 2003 호)
조현룡(경기도 수원시 팔달구 매탄 1 동 주공아파트 5 단지 523 동 908 호)

발 신 : 고려특허법률사무소 오세준(기술)/김연정(관리)

제 목 : 선언서/양도증 서명요청

1. 특허등록현황

국가	미 국	출원종류	PCT 국내단계진입
당소참조번호	XP16327-US		
우선권번호	P2004-18139	국내출원일	2004.3.17
PCT 출원번호	PCT/KR2005/000036	PCT 출원일	2005.01.07
현지 대리인	HDP	국내단계진입일	2006.09.15
미국출원번호	10/593,088		
발 명 자	최번재, 박진수, 김성한, 공명국, 조현룡		
발명 명칭	무반사 처리된 고효율 발광다이오드소자		
선언서/양도증 요청일	2008 년 7 월 9 일		

1. 상기 PCT출원 PCT/KR2005/000036의 2006년 9월 15일자로 미국 국내단계 진입이 완료된 본건의 선언서/양도증 양식을 송부하오니, 발명자 서명과 날짜 기재하셔서 **2008년 7월 9일**까지 당소로 원본(팩스/이메일 가능)을 회송하여 주시기 바랍니다.

2. 본건의 출원서와 선언서/양도증 양식 동봉합니다.

3. 기타 위의 건에 대한 문의사항이 있으시면 기술담당자(오세준) 또는 관리담당자(김연정)앞으로 연락 주시기 바랍니다.

(Tel.02-2186-8314, E-maill:kr@krpatent.co.kr)

고려국제특허법률사무소

※ 첨부서류: 1. 출원서
2. 선언서/양도증

ASSIGNMENT

Atty. Docket No. **8947-000222/US**

WHEREAS, the undersigned, hereinafter referred to collectively as Assignor, has invented:

ANTI-REFLECTED HIGH EFFICIENCY LIGHT EMITTING DIODE DEVICE

for which Assignor is about to make or has made United States or International application for patent

(a) ☐ executed on even date preparatory to filing (each inventor should sign this Assignment on the same day as he/she signs the Declaration and Power of Attorney);

(b) ☐ executed on _____, _____, _____; or

(c) ☒ filed on January 7, 2005, and assigned Serial No. __ or PCT International Application No. PC/KR2005/000036; and

WHEREAS, EPIPLUS CO., LTD., Eyon-Hansan Industrial Park, 1027 Yulbuk-Ri, Chungbuk-Myun, Pyongtaek, Gyeonggi-do 451-833, Republic of Korea, hereinafter referred to as Assignee, is desirous of acquiring all right, title, and interest therein:

NOW, THEREFORE, for good and valuable consideration, the receipt and adequacy whereof is hereby acknowledged, Assignor agrees to, and hereby does, sell, assign and transfer unto Assignee and its successors in interest, the full and exclusive right, title and interest in the United States of America and throughout the world, including the right to claim priority under the laws of the United States, the Paris Convention, and any foreign countries, to the invention as described in the aforesaid application and all United States Letters Patent which may be granted therefore, and all divisions, continuations, reissues, reexaminations and extensions thereof, these rights, title and interest to be held and enjoyed by Assignee to the full end of the term for which the Letters Patent are granted and any extensions thereof as fully and entirely as the same would have been held by Assignor had this assignment and sale not been made, and the right to sue for, and recover for past infringements of, or liabilities for, any of the rights relating to any of the applications or patents resulting therefrom;

Assignor hereby covenants and agrees to execute all instruments or documents required or requested for the making and prosecution of any applications of any type for patent in the United States and in all foreign countries including, but not limited to, any provisional, continuation, continuation-in-part, divisional, renewal or substitute thereof, and as to letters patent any reissue, re-examination, or extension thereof, and for litigation regarding, or for the purpose of protecting title and to the said invention, the United States application for patent, or Letters Patent therefor, and to testify in support thereof, for the benefit of Assignee without further or other compensation than that above set forth;

Assignor hereby covenants that no assignment, sale, license, agreement or encumbrance has been or will be entered into which would conflict with this Assignment; and

Assignor hereby requests the United States Patent and Trademark Office to issue the Letters Patent of the United States of America to Assignee, and requests that any official of any country or countries foreign to the United States, whose duty it is to issue or grant patents and applications as aforesaid, to issue the Letters Patent, Utility Model Registration or Inventor's Certificate to Assignee.

The undersigned hereby grant(s) the law firm of Harness, Dickey & Pierce, P.L.C. the power to insert on this Assignment any further identification which may be necessary or desirable in order to comply with the rules of the U.S. Patent and Trademark Office for recordation of this document.

ASSIGNMENT

Atty. Docket No. **8947-000222/US**

Pun Jae CHOI

Dated

Jin Soo PARK

Dated

Seong Han KIM

Dated

Myeong Kook GONG

Dated

Hyeon Ryong CHO

Dated

Atty. Dkt. No.:8947-000222/US

DECLARATION AND POWER OF ATTORNEY (POA)

As a below named inventor, I hereby declare that:

My residence, mailing address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

ANTI-REFLECTED HIGH EFFICIENCY LIGHT EMITTING DIODE DEVICE

the specification of which (check one)

☐ is attached hereto.
or
☒ was filed on January 7, 2005 as Application Serial No. or PCT International Application No. PCT/KR2005/000036 and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. §§ 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or any PCT international application having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)				
APPN. SERIAL NO.	COUNTRY	DATE FILED (MM/DD/YYYY)	PRIORITY CLAIM	
			Yes	No
10-2004-0018139	KOREA	March 17, 2004	☒	☐
			☐	☐
			☐	☐

Atty. Dkt. No.: 8947-000222/US

DEC. AND POA Cont'd

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

PRIOR PROVISIONAL APPLICATION(S)	
APPN. SERIAL NO.	DATE FILED (MM/DD/YYYY)

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) listed below:

PRIOR U.S. APPLICATION(S)		
APPN. SERIAL NO.	DATE FILED (MM/DD/YYYY)	STATUS - PATENTED, PENDING, ABANDONED

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY

I hereby appoint the following attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

Thomas S. Auchterlonie	Reg. No. 37,275
John A. Castellano	Reg. No. 35,094
Terry L. Clark	Reg. No. 32,644
Donald J. Daley	Reg. No. 34,313
Gary D. Yacura	Reg. No. 35,416

and all individuals assigned to Customer No. **30593**.

Atty. Dkt. No.: 8947-000222/US

DEC. AND POA Cont'd

CORRESPONDENCE ADDRESS

I request the Patent and Trademark Office to direct all correspondence and telephone calls relative to this application to Harness, Dickey & Pierce, P.L.C., Customer No. 30593, P.O. Box 8910, Reston, Virginia, 20195, (703) 668-8000.

Full name of sole or first inventor: Pun-Jae CHOI

Inventor's signature: _____

Date: _____

Residence: 203-1101 Hansol Apt., Songgang-dong, Yuseong-gu, Daejeon KOREA

Citizenship: Republic of Korea

Mailing Address: Same as above

Full name of second joint inventor: Jin-Soo PARK

Inventor's signature: _____

Date: _____

Residence: 629 Beonji, Deongnim-ri, Jusan-myeon, Buan-gun, Jeollabuk-do, KOREA

Citizenship: Republic of Korea

Mailing Address: Same as above

Full name of third joint inventor: Seong-Han KIM

Inventor's signature: _____

Date: _____

Residence: 204-303 Hansol Apt., Songgang-dong, Yuseong-gu, Daejeon, KOREA

Citizenship: Republic of Korea

Mailing Address: Same as above

Atty. Dkt. No.: 8947-000222/US

DEC. AND POA Cont'd

Full name of fourth joint inventor: Myeong-Kook GONG

Inventor's signature: _____

Date: _____

Residence: 901-2003 LG-XI Apt., 869 Beonji, Sanghyeon-dong, Yongin, Gyeonggi-do KOREA

Citizenship: Republic of Korea

Mailing Address: Same as above

Full name of fifth joint inventor: Hyeon-Ryong CHO

Inventor's signature: _____

Date: _____

Residence: 523-908 5 Danji Jugong Apt., Maetan 1-dong, Paldal-gu, Suwon, Gyeonggi-do KOREA

Citizenship: Republic of Korea

Mailing Address: Same as above

HARNESS DICKEY

John Castellano
Direct Dial: 703-668-8029
jcastellano@hdp.com

CONFIDENTIAL AND PRIVILEGED COMMUNICATION OF COUNSEL

September 15, 2006

VIA FACSIMILE & AIRMAIL
011-82-2-2186-8301

Mr. Hyuk-Soo Kwon
KORYO INTERNATIONAL PATENT & LAW OFFICE
SL. Kang Nam
P.O. Box 1132
Seoul 135-611
REPUBLIC OF KOREA

Re: Inventor(s): Pun Jae CHOI et al. – ***Filed: September 15, 2006***
Title: "ANTI-REFLECTED HIGH EFFICIENCY LIGHT EMITTING DIODE DEVICE"
Your Ref.: XP16327-US - Our Ref.: 8947-000222/US

Dear Mr. Kwon:

Further to your letter of September 14, 2006, this is to advise you that we filed the above-identified U.S. National Phase application on even date herewith in the U.S. Patent and Trademark Office. Enclosed herewith are copies of these papers as filed for your information and records. The items filed with the U.S. Patent and Trademark Office are as follows:

PCT Transmittal
Preliminary Amendment (6 pages)
Information Disclosure Statement
PTO-1449 Form w/ Listing Four (4) References, Enclosing One (1) ISR, IPER
International Application as Filed
Formal Drawings (5 sheets)

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	NEW APPLICATION
International App. No.:	PCT/KR2005/000036
Filing Date:	September 15, 2006
Applicant:	Pun Jae CHOI et al.
Group Art Unit:	Unknown
Examiner:	Unknown
Title:	ANTI-REFLECTED HIGH EFFICIENCY LIGHT EMITTING DIODE DEVICE
Attorney Docket:	8947-000222/US

PRELIMINARY AMENDMENT

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

September 15, 2006

Sir:

The following preliminary amendments and remarks are respectfully submitted in connection with the above-identified application. Prior to examination of the present application, please consider the following:

Amendments to the Claims begin on page 2 of this Preliminary Amendment.

Remarks begin on page 5 of this Preliminary Amendment.

IN THE CLAIMS

This is a complete and current listing of the claims, marked with status identifiers in parentheses. The following listing of claims will replace all prior versions and listings of claims in the application.

Claims

1. (Previously Presented) A light emitting diode including a substrate, a N-type semiconductor layer, an active layer for generating light, and a P-type semiconductor layer, the light emitting diode comprising:

a first exposed region formed by etching the active layer and the P-type semiconductor layer to expose at least a part of the N-type semiconductor layer;

a first ohmic electrode formed on the first exposed layer;

a second ohmic electrode formed on the P-type semiconductor layer and having an opening at least a part of said P-type semiconductor layer having a second exposed region through said opening; and

said at least a part of P-type semiconductor layer being provided with an ultra-fine prominence and depression structure.

2. (Previously Presented) The light emitting diode as claimed in claim 1, wherein at least a part of the first exposed region excepting a portion having the first ohmic electrode has an ultra-fine prominence and depression structure.

3. (Previously Presented) A light emitting diode including a substrate, a N-type semiconductor layer, an active layer for generating light, a P-type semiconductor layer, a transparence metal (electrode), and a metal pad for wire bonding the light emitting diode comprising:

a first exposed region formed by etching the active layer and the P-type semiconductor layer to expose at least a part of the N-type semiconductor layer;

a first ohmic electrode formed on the first exposed layer; and

at least a part of said first exposed region excepting a portion having the first ohmic electrode being provided with an ultra-fine prominence and depression structure.

4. (Currently Amended) The light emitting diode as claimed in ~~any one of~~ claims 1~~—3~~, wherein the P-type semiconductor layer is GaN doped with Mg the N-type semiconductor layer is GaN doped with Si, and the active layer is GaN.

5. (Currently Amended) The light emitting diode as claimed in ~~any one of~~ claims 1~~—3~~, wherein the ultra-fine prominence and depression structure is a cluster of cylinder type prominence and depression elements.

6. (Previously Presented) The light emitting diode as claimed in claim 5, wherein the cylinder type prominence and depression element is a cone type, a column type, or a column type having a depressed upper end.

7. (Previously Presented) The light emitting diode as claimed in claim 5, wherein a width of the cylinder type prominence and depression element is 0.005 ~ 3 μm , and a height is 0.1 ~ 1 μm.

8 (Previously Presented) The light emitting diode as claimed in claim 5, wherein a width of the cylinder type prominence and depression element is 0.01 ~ 0.5 μm , and a height is 0.2 ~ 0.7 μm.

9. (Previously Presented) The light emitting diode as claimed in claim 5, wherein a width of the cylinder type prominence and depression element is 0.01 ~ 2 times larger than a peak wavelength of the light emitting diode, and a height is 0.5 ~ 10 times larger than the peak

wavelength.

10. (Previously Presented) The light emitting diode as claimed in claim 5, wherein a width of the cylinder type prominence and depression element is 0.1 ~ 1 times larger than a peak wavelength of the light emitting diode, and a height is 1 ~ 3 times larger than the peak wavelength.

11. (Previously Presented) The light emitting diode as claimed in claim 5, wherein a density of the cylinder type prominence and depression elements is 1 ~ 10000/ μm^2.

12. (Previously Presented) The light emitting diode as claimed in claim 5, wherein a density of the cylinder type prominence and depression elements is 50 ~ 500/ μm^2.

13. (Previously Presented) The light emitting diode as claimed in claim 5, wherein the cylinder type prominence and depression element is formed by depositing a metal or silicon compound on the semiconductor layer, heat-treating the deposited metal or silicon compound, and dry- or wet-etching the deposited metal or silicon compound.

14. (Previously Presented) The light emitting diode as claimed in claim 13, wherein the metal is any one or combinations selected from a group of Ag Al, Au, Cr, In, Ni, Pd, Pt and Ti.

15. (Previously Presented) The light emitting diode as claimed in claim 13, wherein a temperature for the heat-treating is ranged from 90 °C to 400 °C.

16. (Previously Presented) The light emitting diode as claimed in claim 15, wherein the cylinder type prominence and depression element is formed by selectivity, said selectivity being partly changed due to a reaction of the metal and the semiconductor at time of etching.

REMARKS

It should be noted that the amendments to original claims 1-16 of the present application are non-narrowing amendments, made solely to place the claims in proper form for U.S. practice and not to overcome any prior art or for any other statutory considerations. Other amended claims have been made to broaden the claims; remove multiple dependencies in the claims; remove/change any phrases unique to European practice; and to place claims in a more recognizable U.S. form. Other such non-narrowing amendments include placing apparatus-type claims (setting forth elements in separate paragraphs) in a more recognizable U.S. form. Again, all amendments are non-narrowing and have been made solely to place the claims in proper form for U.S. practice and not to overcome any prior art or for any other statutory considerations.

CONCLUSION

Accordingly, in view of the above amendments and remarks, an early indication of the allowability of each of claims 1-16 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY & PIERCE, P.L.C

By: _____
John A. Castellano, Reg. No. 35,094

P.O. Box 8910
Reston, Virginia 20195
(703) 668-8000

JAC:dpg

PATENT
8947-000222/US

IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicant(s):	Pun Jae CHOI et al.
Int'l Application No.:	PCT/KR2005/000036
Application No.:	**NEW**
Filed:	September 15, 2006
For:	ANTI-REFLECTED HIGH EFFICIENCY LIGHT EMITTING DIODE DEVICE

INFORMATION DISCLOSURE STATEMENT (SUBMISSION CONCURRENT WITH THE FILING OF A NEW PATENT APPLICATION)

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314
Mail Stop PCT

September 15, 2006

Sir:

Pursuant to 37 C.F.R. §§ 1.97 and 1.98, applicant(s) hereby submit(s) an Information Disclosure Statement for consideration by the Examiner.

I. LIST OF PATENTS, PUBLICATIONS OR OTHER INFORMATION

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FEES

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Respectfully submitted,

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Enclosures:

- ☒ Form PTO-1449(s)
- ☒ Documents
- ☒ International Search Report (PCT/ISA/210 and PCT/ISA/220)
- ☒ International Preliminary Examination Report (PCT/IPEA/416 and PCT/IPEA/409)
- ☐ Fee

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

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APPLICANTS	CONF. NO.
Pun Jae CHOI et al.	Unknown
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	US 2001/0048113 A1	12/6/2001	Kim			
	US 6,504,180 B1	1/7/2003	Heremans			
	US 2003/0062530 A1	4/3/2003	Toshiba			

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION	
						YES	NO
	KR 2005-0003671 A	1/12/2005	KOREA				

OTHER DOCUMENTS

(Include Name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.

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Description

ANTI-REFLECTED HIGH EFFICIENCY LIGHT EMITTING DIODE DEVICE

Technical Field

[1] The present invention relates to a light emitting diode, and in particular, relates to an anti-reflected light emitting diode having an ultra-fine prominence and depression to increase a light extraction efficiency.

Background Art

[2] Generally, a light emitting diode(hereafter referred as 'LED') is a kind of solid-state device for converting an electric energy to light, and have two semiconductor layers(N-type, and P-type) oppositely doped with each other and an active layer positioned between the layers. When a bias is applied to the two semiconductor layers, holes and electrons are injected into the active layer to be recombined to generate light. The light generated in the active region is omnidirectionally emitted, and a part of the light is emitted to the outside of semiconductor chip through a surface exposed to the outside.

[3] Recently, as the material for semiconductor is improved, the efficiency of semiconductor chip is also increased. New type LED is made of GaN group material to permit an efficient illumination in a spectrum from ultraviolet ray to green ray. As the LED is improved, the LED is expected to substitute prior art lighting used in a traffic signal lamp, an indoor or outdoor display, a headlight and a tail-light for vehicle, and prior art indoor lighting device. However, the prior art LED cannot emit all the light generated in the active layer. Thus, the efficiency is restricted.

[4] Fig. 1 is a cross-sectional view of prior art light emitting diode provided with a mesh-type ohmic contact. After a N-type semiconductor layer 20, an active layer 30, and a P-type semiconductor layer 40 are in sequence deposited on a substrate 10, a mesh-type ohmic contact 50b is formed. The mesh-type is a structure having openings through which a part of the N-type semiconductor layer 40 is exposed. If, the ohmic electrode 50b having openings is not formed on the P-type semiconductor layer and, instead, a transparence metal(PT) is formed on the layer, a part of light generated in the active layer 30 is reflected at the P-type semiconductor layer 40 and the transparence metal. Even though a part of light is passed through the transparence metal, as the light is a degree of 400 nm of visual ray, a boundary condition is not satisfied in the thin transparence metal having a thickness of a few nm ~ several tens

nm to occur a loss of light. Therefore, by applying the ohmic electrode 50b having the openings, the light generated in the active layer is passed to the air through the openings, or through the openings and an epoxy resin to reduce the loss of light.

[5] The LED provided with the ohmic electrode 50b has a problem. The typical refractive index of semiconductor material is about 2.2 ~ 3.8, which is higher than that of the air(n=1.0) and encapsulating epoxy(n ≒ 1.5). According to Snell's law, a light, with an angle larger than a critical angel, moved from a region with high refractive index to a region with low refractive index is not passed to the outside and is totally reflected to the inside(that is, Total Internal Reflection : TIR). Therefore, a part of light emitted from the active layer 30 cannot be passed through a surface, in contact with the air or the epoxy, of the P-type semiconductor layer 40 and is totally reflected to the inside at the surface. The reflected light continues reflections until absorbed in the LED, or is emitted to the outside through other surfaces. Thus, there is a problem that a light extraction efficiency is lowed in the light emitting diode with the mesh-type ohmic electrode.

Disclosure of Invention

Technical Solution

[6] Therefore, an object of the present invention is to solve the problems involved in the prior art, and to provide a light emitting diode in which a light generated is not reflected from a semiconductor layer having an ultra-fine prominence and depression structure and is emitted to the outside to increase a light extraction efficiency.

[7] According to one embodiment of the present invention, in a light emitting diode having a substrate, a N-type semiconductor layer, an active layer for generating light and a P-type semiconductor layer, the light emitting diode further comprises: a first exposed region formed by etching the active layer and the P-type semiconductor layer to partly expose the N-type semiconductor layer; a first ohmic electrode formed on the first exposed region; and a second ohmic electrode formed on the P-type semiconductor layer, and having an opening to partly form a second exposed region on the P-type semiconductor layer. At least a part of the second exposed region is formed to have an ultra-fine prominence and depression.

[8] Preferably, at least a part of the first exposed region excepting a portion having the first ohmic electrode has a prominence and depression structure.

[9] According to other embodiment of the present invention, in a light emitting diode having a substrate, a N-type semiconductor layer, an active layer for generating light, a P-type semiconductor layer, a transparence metal(electrode), and a metal pad for wire

bonding, the light emitting diode further comprises: a first exposed region formed by etching the active layer and the P-type semiconductor layer to expose at least a part of the N-type semiconductor layer; and a first ohmic electrode formed on the first exposed region. At least a part of the first exposed region excepting a portion having the first ohmic electrode is formed to have an ultra-fine prominence and depression.

[10] In the embodiments, the P-type semiconductor layer is preferably GaN doped with Mg, the N-type semiconductor layer is preferably GaN doped with Si, and the active layer is preferably GaN.

[11] In the embodiments, the ultra-fine prominence and depression is preferably a cluster of a cylinder shaped prominence and depression elements.

[12] In the embodiments, the cylinder shaped prominence and depression element is substantially a cone type, a column type, or a cylinder having the depressed upper end.

[13] In the embodiments, the width of the prominence and depression element is preferably 0.005 ~ 3μm, and more preferably 0.01 ~ 0.5μm. The height of the prominence and depression element is preferably 0.1 ~ 1μm, and more preferably 0.2 ~ 0.7μm.

[14] In the embodiments, the width of the prominence and depression element is 0.01 ~ 2 times larger than a peak wavelength of light emitted from the light emitting diode, and more preferably 0.1 ~ 1 times larger. The height of the prominence and depression element is 0.5 ~ 10 times larger than the peak wavelength of light emitted from the light emitting diode, and more preferably 1 ~ 3 times larger.

[15] In the embodiments, the density of the prominence and depression elements is preferably 1 ~ 10000/μm^2, and more preferably 50 ~ 500/μm^2.

[16] According to the embodiments, the light extraction efficiency can be increased.

Description of Drawings

[17] The above objects, other features and advantages of the present invention will become more apparent by describing the preferred embodiment thereof with reference to the accompanying drawings, in which:

[18] Fig. 1 is a cross-sectional view of prior art light emitting diode provided with a mesh-type ohmic contact;

[19] Fig. 2 is a schematic perspective view of a light emitting diode according to one embodiment of the present invention;

[20] Fig. 3 is a cross-sectional view taken along line S1 in Fig. 2;

[21] Fig.4 is a cross-sectional view of a light emitting diode according to other embodiment of the present invention;

[22] Fig. 5 is a diagram showing various examples of a discrete prominence and depression element used in an ultra-fine prominence and depression structure formed on a light emitting diode according to the present invention;

[23] Fig. 6 is an enlarged picture showing an ultra-fine prominence and depression structure of high density;

[24] Fig. 7 is an enlarged picture showing an ultra-fine prominence and depression structure of low density;

[25] Fig. 8 is an enlarged picture showing a thick ultra-fine prominence and depression structure;

[26] Fig. 9 is an enlarged picture showing thin ultra-fine prominence and depression structure;

[27] Fig. 10 and 11 are schematic diagrams showing an ultra-fine prominence and depression structure formed on a light emitting diode according to the present invention; and

[28] Fig. 12 is a graph illustrating the characteristic of optical power of a light emitting diode according to the present invention.

[29] *Brief Description of reference number*

[30] 10: light-permeable sapphire substrate A1: first exposed region

[31] 20: N-type semiconductor layer A2: second exposed region

[32] 30: active layer 60: transparence metal

[33] 40: P-type semiconductor layer 70: metal pad for wire bonding

[34] 50a: first ohmic electrode 80: air

[35] 50b: second ohmic electrode

Best Mode

[36] Reference will now be made in detail to an anti-reflected high efficiency light emitting diode device according to the present invention by using the accompanying drawings. In the following explanation, a description through accompanying drawings will be added in order to facilitate further complete understanding of the present invention, but it is apparent to those skilled in the art that the present invention can be carried out without a detailed description of the drawings. In cases, a description of the main elements or constituents of the known technology will be omitted if it obscures the point of the present invention unnecessarily. This is intended to avoid any possibility to obscure the description of the present invention.

[37] Fig. 2 is a schematic perspective view of a light emitting diode according to one embodiment of the present invention, and Fig. 3 is a cross-sectional view taken along

line S1 in Fig. 2.

[38] With reference to Fig. 2 and Fig. 3, in order to realize the present invention, a N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor 40 are in sequence formed on a substrate 10 by using an epitaxial process. The substrate 10 can be a light-permeable sapphire substrate. The N-type semiconductor layer 20 is formed by GaN(Gallium Nitride) doped with Si, but not restricted to the same. The P-type semiconductor layer 40 is formed by GaN doped with Mg but not restricted to the same. The active layer 30 formed by one selected from GaN, AlGaN and InGaN, and the amount of the Al and the In can be adjusted according to a kind of light generated in the active layer.

[39] Next, a part of the active layer 30 and the P-type semiconductor layer 40 is etched by using a photo lithography process to expose the N-type semiconductor layer 20. Then, a first exposed region A1 is formed on the N-type semiconductor layer 20. Preferably, the first exposed region A1 is formed on the margin portions of the N-type semiconductor layer 20 by etching the edge portions of the active layer 30 and P-type semiconductor layer 40. Then, a first rectangular shaped ohmic electrode 50a is formed on one of the margin portions of the N-type semiconductor layer 20 by etching the active layer 30 and the P-type semiconductor layer 40.

[40] Next, an ultra-fine prominence and depression structure is formed on the first exposed region A1 excepting the portion having the first ohmic electrode 50a, and on a second exposed region A2. The reason why the ultra-fine prominence and depression structure is formed is to emit the light generated in the active layer 30 to outside without a reflection in the first exposed region A1 and the second exposed region A2. The structure of prominence and depression and method for forming the same will be described later with reference to Fig. 5 - Fig. 9. The second exposed region A2 is an exposed portion of the P-type semiconductor layer 40 excepting a portion having a second ohmic electrode 50b thereon. The exposed region includes portions exposed through openings of the second ohmic electrode 50b.

[41] After forming the prominence and depression on the N- and the P-type semiconductor layers, the first ohmic electrode 50a is formed on a part of the first exposed region A1, and the second ohmic electrode 50b is formed on the P-type semiconductor layer 40 through a photo lithography process.

[42] As the ultra-fine prominence and depression structure is not formed under the first ohmic electrode 50a and the second ohmic electrode 50b, the under surfaces of the first and the second ohmic electrodes 50a and 50b maintain smoothness. The material for

the ohmic electrodes 50a and 50b is selected from any one of Ti, Al, Au, Ni, Pt, Pd, Ag Rh or compound of the elements. If a white metal such as Al, Pt and Cr is used, the reflexibility of the under surfaces can be increased.

[43] In above description, the method for forming the ultra-fine prominence and depression structure on the N-type semiconductor layer 20 and the P-type semiconductor layer 40 excepting the portions having the ohmic electrodes 50a and 50b thereon before forming the ohmic electrodes 50a and 50b. However, the ultra-fine prominence and depression structure can be formed on the N-type semiconductor layer 20 and the P-type semiconductor layer 40 excepting the portions having the ohmic electrodes 50a and 50b thereon after forming the ohmic electrodes 50a and 50b. In this case, the ohmic electrodes function as a self-aligner.

[44] According to the embodiment, as the light generated in the active layer 30 is not reflected into the inside of the active layer by the ultra-fine prominence and depression structure which is formed on the first exposed region A1 excepting the portion having ohmic electrode 50a and on the second exposed regions A2, the light extraction efficiency of the light emitting diode is increased.

[45] Fig. 4 is a cross-sectional view of a light emitting diode according to other embodiment of the present invention. When comparing the light emitting diode in Fig. 4 with that of Fig. 3, a ultra-fine prominence and depression structure is not formed on the P-type semiconductor layer, and a light permeable electrode(transparence metal) 60 and a metal pad 70 for wire bonding are instead formed on the P-type semiconductor layer in Fig. 4. An ultra-fine prominence and depression structure is formed on the first exposed region A1 of the N-type semiconductor layer 20 excepting the portion having the ohmic electrode 50a as is in Fig. 3.

[46] According to the embodiment, the light generated in the active layer, which is projected into the P-type semiconductor layer 40 with an incidence angle larger than a critical angle, is totally reflected to the inside by the light permeable electrode 60, and to be projected into the N-type semiconductor layer 20. The light projected into the N-type semiconductor layer is reflected again at the bottom of the layer to be emitted to the outside of the layer through the exposed region A1 without a refection.

[47] Further, in the embodiment, as the first ohmic electrode 50a is formed to have a smooth bottom surface as is in Fig. 3, the light projected to the bottom surface is reflected to the inside and emitted to the outside to increase the light extraction efficiency.

[48] Fig. 5 is a diagram showing various example of a discrete prominence and

depression element used in an ultra-fine prominence and depression structure formed on a light emitting diode according to the present invention.

[49] The ultra-fine prominence and depression structure is a cluster of a cylinder shaped prominence and depression elements having a few ?(Angstrom) ~ a few nm(nano-meter) dimensions . Each of the prominence and depression elements has a different size and shape. The width(w) of the discrete prominence and depression element is about 0.005 ~ 3μm, and preferably 0.01 ~ 0.5μm. The height of the discrete prominence and depression element is about 0.1 ~ 1μm, and preferably 0.2 ~ 0.7μm.

[50] The dimension(width or height) of the prominence and depression element is similar to that of a peak wavelength(λp) of light generated in the light emitting diode. The width(w) of the prominence and depression element is 0.01 ~ 2 times larger than the peak wavelength of light, and preferably 0.1 ~ 1 times. The height of the prominence and depression element is 0.5 ~ 10 times larger than the peak wavelength of light, and preferably 1 ~ 3 times larger.

[51] As shown in Fig. 5, the discrete prominence and depression element has various shapes. The shape of the element is generally a cylinder type protruded from the semiconductor layers 20 and 40. More detail, the shape is similar to a cone or a column, or is a column having a depressed upper end. A small number of ruggedness ~ tens of thousands of ruggedness much smaller than the prominence and depression element can be formed on the depressed upper end.

[52] Fig. 6 ~ Fig. 9 are enlarged pictures showing a prominence and depression structure formed on a light emitting diode according to the present invention. Fig. 6 shows a prominence and depression structure of high density, Fig. 7 shows a prominence and depression structure of low density, Fig. 8 shows a thick prominence and depression structure, and Fig. 9 shows a thin prominence and depression structure.

[53] The term 'density' used in here means the number of the prominence and depression element per the unit area[unit/μm]. The term 'high density' means that numbers of ruggedness are densely formed. The density of the prominence and depression elements is about 1 ~ 10000/ μm^2, and more preferably 50 ~ 5000/μm^2.

[54] The term 'thick' means that the height(h) is smaller than the width(w).

[55] There are various methods for forming the prominence and depression structure on the semiconductor layers 20 and 40. In one method, a metal cluster is formed by depositing a metal(Ag, Al, Au, Cr, In, Ir, Ni, Pd, Pb, Pt, Rd, Sn, Ti, W, or a compound of the elements) on the first exposed region A1 of the N-type semiconductor layer 20 and on the P-type semiconductor layer 40 and heat-treating the metal in high

temperature. Next, the metal cluster in a portion to be formed with the first ohmic electrode 50a in the first exposed region and in a portion to be formed with the second ohmic electrode 50b in the P-type semiconductor layer 40 is removed by a photo lithography process. Next, the ultra-fine prominence and depression structure is formed by dry- or wet-etching the rest of metal cluster on the first exposed region A1 excepting the portion to be formed with the first ohmic electrode 50a and on the second exposed region A2.

[56] In other method, the prominence and depression structure is formed by etching the first exposed region A1 excepting the portion to be formed with the first ohmic electrode 50a, and the second exposed region A2 using ICP and RIE through a photo lithography process, after growing roughly a silicon compound such as SiO_2 and Si_3N_4 on the exposed regions by using a porous growing method.

[57] Further, after growing silicon compound such as SiO_2 and Si_3N_4, and forming a metal cluster by depositing a metal(Ag, Al, Au, Cr, In, Ir, Ni, Pd, Pb, Pt, Rd, Sn, Ti, W or a compound of elements) on the silicon compound and heat-treating the deposited metal in high temperature, the prominence and depression structure is formed by selectively (wet or dry)etching the metal cluster on the first exposed region A1 excepting the portion to be formed with the first ohmic electrode 50a, and the second exposed region A2 through a photo lithography process.

[58] The examples for forming the prominence and depression structure on the semiconductor layers 20 and 40 by using the methods are as follow.

[59] [Example 1] High Density, Thin type

[60] Type : Thin type (Width(w) : about 0.01 ~ 0.03μm/ Height(h):about 0.5μm)

[61] Density : about 40 ~ 70/μm^2

[62] Used Metal : Ni, Au(20? ~ 50?) (or In, Au and Ni compound used)

[63] Heat treating : 550 ℃ ~ 650 ℃ for 60sec ~ 120sec

[64] Dry etching : ICP treating for 300sec

[65] [Example 2] High Density, Thick type

[66] Type : Thick type (Width(w) : about 0.08 ~ 0.15μm/ Height(h):about 0.5μm)

[67] Density : about 40 ~ 70/μm^2

[68] Used Metal : Ni, Au(50? ~ 100?) (or In, Au and Ni compound used)

[69] Heat treating : 550 ℃ ~ 650 ℃ for 60sec ~ 120sec

[70] Dry etching : ICP treating for 300sec

[71] [Example 3] Low Density, Thin type

[72] Type : Thin type (Width(w) : about 0.01 ~ 0.03μm/ Height(h):about 0.5μm)

[73] Density : about 4 ~ 8/μm^2

[74] Used Metal : Ni, Au(20? ~ 50?) (or In, Au and Ni compound used)

[75] Heat treating : 500 ℃ ~ 600 ℃ for 20sec ~ 30sec

[76] Dry etching : ICP treating for 300sec

[77] [Example 1] High Density, Thin type, Low Height

[78] Type : Thin type (Width(w) : about 0.08 ~ 0.15μm/ Height(h):about 0.3μm)

[79] Density : about 40 ~ 70/μm^2

[80] Used Metal : Ni, Au(50? ~ 100?) (or In, Au and Ni compound used)

[81] Heat treating : 550 ℃ ~ 650 ℃ for 60sec ~ 120sec

[82] Dry etching : ICP treating for 300sec

[83] Fig. 10 and Fig. 11 are schematic diagrams showing an ultra-fine prominence and depression structure formed on a light emitting diode according to the present invention. With reference to Fig. 10a, there are three layers in the Fig. That is, a semiconductor layer N2, an ultra-fine prominence and depression structure layer Ng and air layer are in the Fig. The ultra-fine prominence and depression structure is formed on the semiconductor layers 20 and 40, and the surface of the prominence and depression structure is in contact with air. The surface can also be in contact with an epoxy resin.

[84] As described above, each of the prominence and depression elements making up the prominence and depression structure has a width of 0.01 ~ 0.5μm and a height of 0.2 ~ 0.7μm, which are about 0.1 ~ 1 times larger than the peak wavelength(p λ).

[85] If the dimensions(w, h) of the prominence and depression element making up the prominence and depression structure is made to have a value similar to a wavelength of light generated in the active layer, a refractive index n_{eff} of the ultra-fine prominence and depression structure is changed in linear from a refractive index n_2 of the semiconductor layer N2 to a refractive index n_1 of the air layer N2. The semiconductor layer N2, the ultra-fine prominence and depression layer Ng and the air layer N1 can be conceptually represented as in Fig. 11.

[86] As the refractive index is linearly changed along the arrow Z, discontinuity of refractive index, that is boundary, is not present. As the boundary is not present, TIR(Total Internal Reflection) phenomenon is not occurred at the boundary. In the result, as a reflection is not occurred in the ultra-fine prominence and depression layer Ng the ultra-fine prominence and depression layer Ng functions a Anti-reflection layer.

[87] As the theoretical description for the light characteristic in case of a structure

smaller than the wavelength of light being in a medium plane is disclosed in 'The optical properties of artificial media structured at a subwavelength scale, Encyclopedia of Optical Engineering, pp. 62-71, 2003', detailed description will be omitted.

[88] As the semiconductor layers 20 and 40 are treated to have the anti-reflection layer, all of light generated in the active layer is emitted from the semiconductor layers 20 and 40 to the outside to increase the light extraction efficiency.

[89] Fig. 12 is a graph illustrating the characteristic of optical power of the light emitting diode according to the present invention. As shown in Fig. 12, the optical power of the light emitting diode according to the present invention is much higher than that of prior art light emitting diode.

[90] The optical power is different from embodiment to embodiment. As the height of the prominence and depression element and the density increase, the effect of the anti reflection can be increased.

[91] While the present invention has been described and illustrated herein with reference to the preferred embodiments thereof, it will be apparent to those skilled in the art that various modifications and variations can be made therein without departing from the spirit and scope of the invention. Thus, it is intended that the present invention covers the modifications and variations of this invention that come within the scope of the appended claims and their equivalents.

Industrial Applicability

[92] According to another aspect of the present invention, as the light extraction efficiency and the light generating efficiency are increased, a light emitting diode with high brightness can be fabricated.

[93] According to other aspect of the present invention, a current supply can be smoothly done by employing a mesh-type ohmic contact having the opening to increase the light generating efficiency.

[94] According to another aspect of the present invention, as the light extraction efficiency and the light generating efficiency are increased, a light emitting diode with high brightness can be fabricated.

Claims

[1] 1. A light emitting diode including a substrate, a N-type semiconductor layer, an active layer for generating light, and a P-type semiconductor layer, the light emitting diode comprising:
a first exposed region formed by etching the active layer and the P-type semiconductor layer to expose at least a part of the N-type semiconductor layer;
a first ohmic electrode formed on the first exposed layer;
a second ohmic electrode formed on the P-type semiconductor layer and having an opening, at least a part of said P-type semiconductor layer having a second exposed region through said opening; and
said at least a part of P-type semiconductor layer being provided with an ultra-fine prominence and depression structure.

2. The light emitting diode as claimed in claim 1, wherein at least a part of the first exposed region excepting a portion having the first ohmic electrode has an ultra-fine prominence and depression structure.

3. A light emitting diode including a substrate, a N-type semiconductor layer, an active layer for generating light, a P-type semiconductor layer, a transparence metal(electrode), and a metal pad for wire bonding, the light emitting diode comprising:
a first exposed region formed by etching the active layer and the P-type semiconductor layer to expose at least a part of the N-type semiconductor layer;
a first ohmic electrode formed on the first exposed layer; and
at least a part of said first exposed region excepting a portion having the first ohmic electrode being provided with an ultra-fine prominence and depression structure.

4. The light emitting diode as claimed in any one of claims 1 - 3, wherein the P-type semiconductor layer is GaN doped with Mg, the N-type semiconductor layer is GaN doped with Si, and the active layer is GaN.

5. The light emitting diode as claimed in any one of claims 1 - 3, wherein the ultra-fine prominence and depression structure is a cluster of cylinder type prominence and depression elements.

6. The light emitting diode as claimed in claim 5, wherein the cylinder type prominence and depression element is a cone type, a column type, or a column type having a depressed upper end.

7. The light emitting diode as claimed in claim 5, wherein a width of the cylinder type prominence and depression element is 0.005 ~ 3 ㎛ , and a height is 0.1 ~ 1 ㎛ .

8 The light emitting diode as claimed in claim 5, wherein a width of the cylinder type prominence and depression element is 0.01 ~ 0.5 ㎛ , and a height is 0.2 ~ 0.7 ㎛ .

9. The light emitting diode as claimed in claim 5, wherein a width of the cylinder type prominence and depression element is 0.01 ~ 2 times larger than a peak wavelength of the light emitting diode, and a height is 0.5 ~ 10 times larger than the peak wavelength.

10. The light emitting diode as claimed in claim 5, wherein a width of the cylinder type prominence and depression element is 0.1 ~ 1 times larger than a peak wavelength of the light emitting diode, and a height is 1 ~ 3 times larger than the peak wavelength.

11. The light emitting diode as claimed in claim 5, wherein a density of the cylinder type prominence and depression elements is 1 ~ 10000/ $㎛^2$.

12. The light emitting diode as claimed in claim 5, wherein a density of the cylinder type prominence and depression elements is 50 ~ 500/ $㎛^2$.

13. The light emitting diode as claimed in claim 5, wherein the cylinder type prominence and depression element is formed by depositing a metal or silicon compound on the semiconductor layer, heat-treating the deposited metal or silicon compound, and dry- or wet-etching the deposited metal or silicon compound.

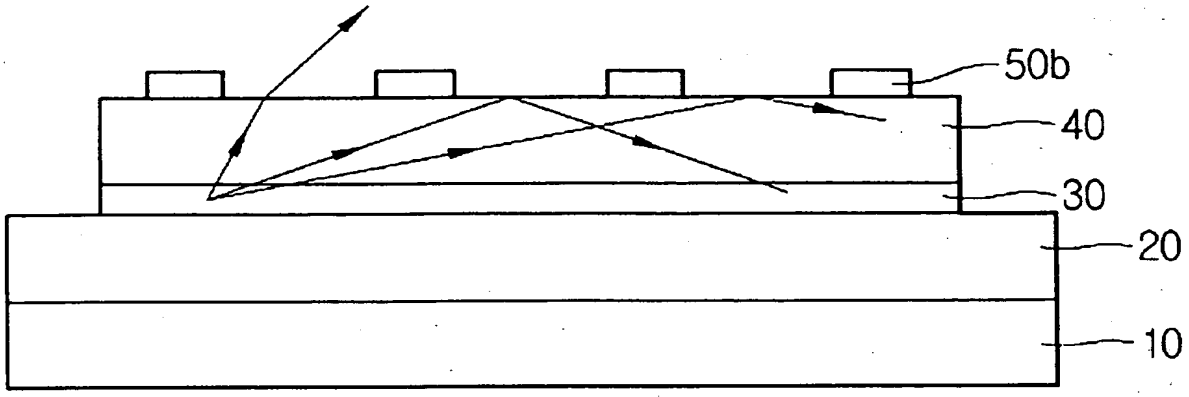
14. The light emitting diode as claimed in claim 13, wherein the metal is any one or combinations selected from a group of Ag, Al, Au, Cr, In, Ni, Pd, Pt and Ti.

15. The light emitting diode as claimed in claim 13, wherein a temperature for the heat-treating is ranged from 90 ℃ to 400 ℃ .

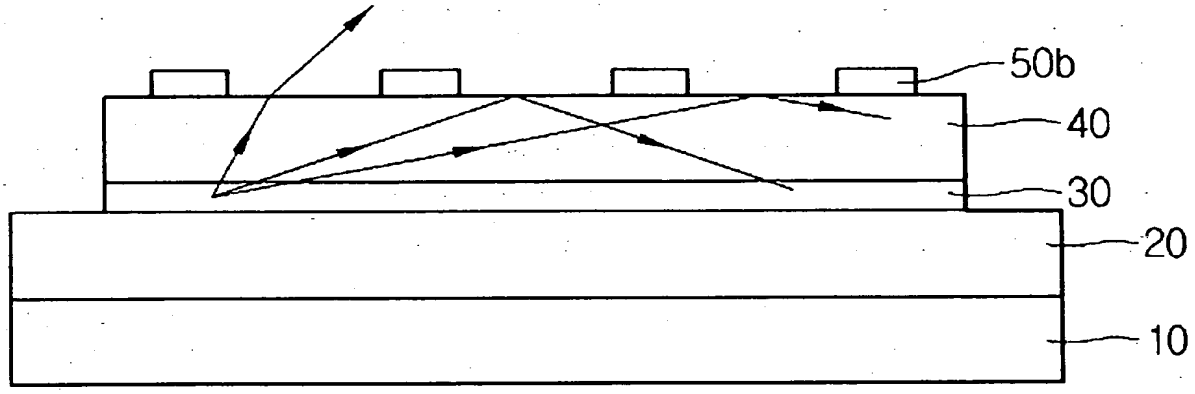
16. The light emitting diode as claimed in claim 15, wherein the cylinder type prominence and depression element is formed by selectivity, said selectivity being partly changed due to a reaction of the metal and the semiconductor at time of etching.

WO 2005/088741 PCT/KR2005/000036

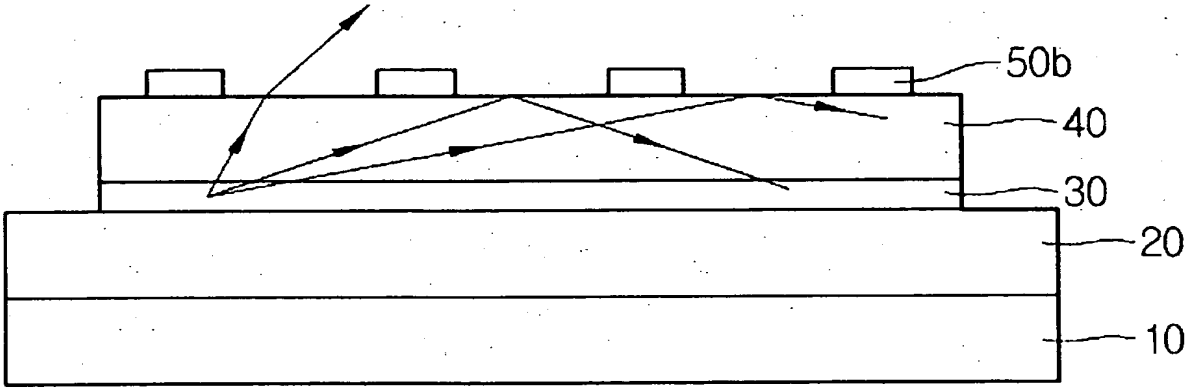
[Fig. 1]



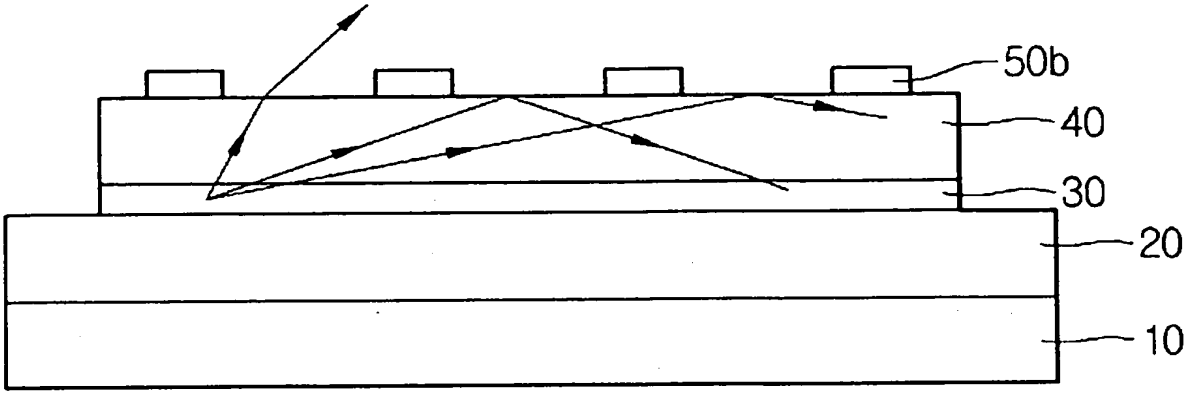
[Fig. 2]



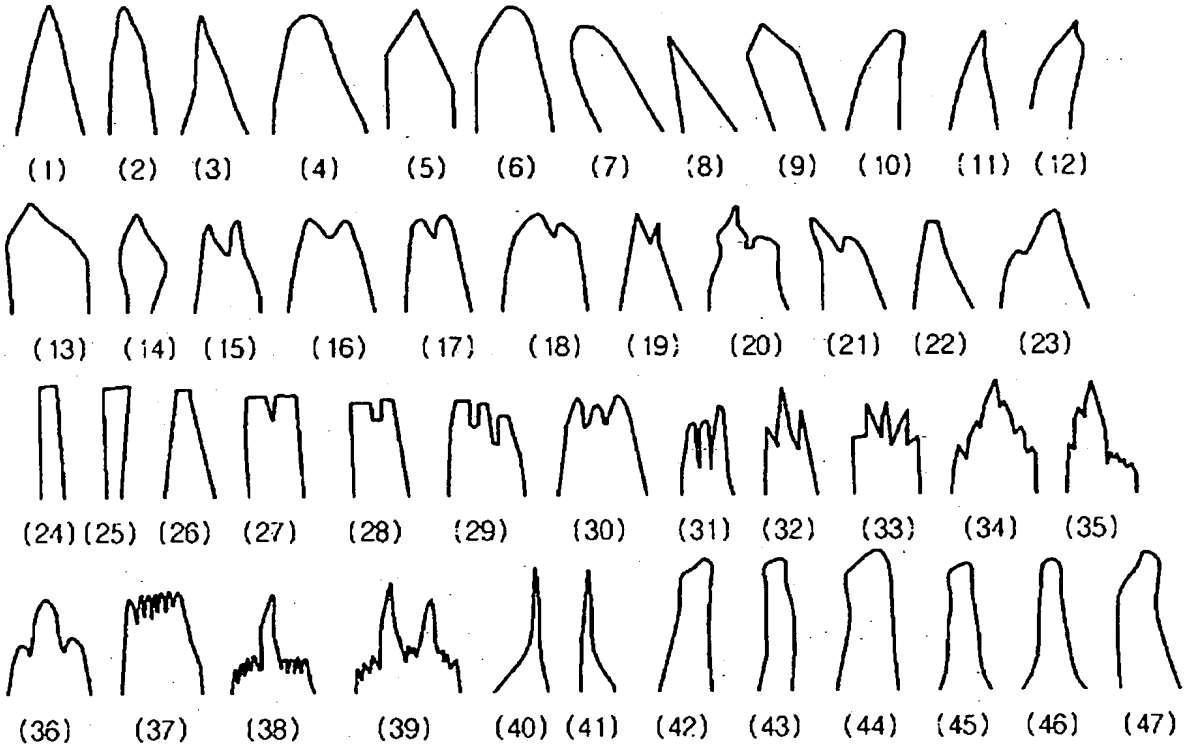
[Fig. 3]



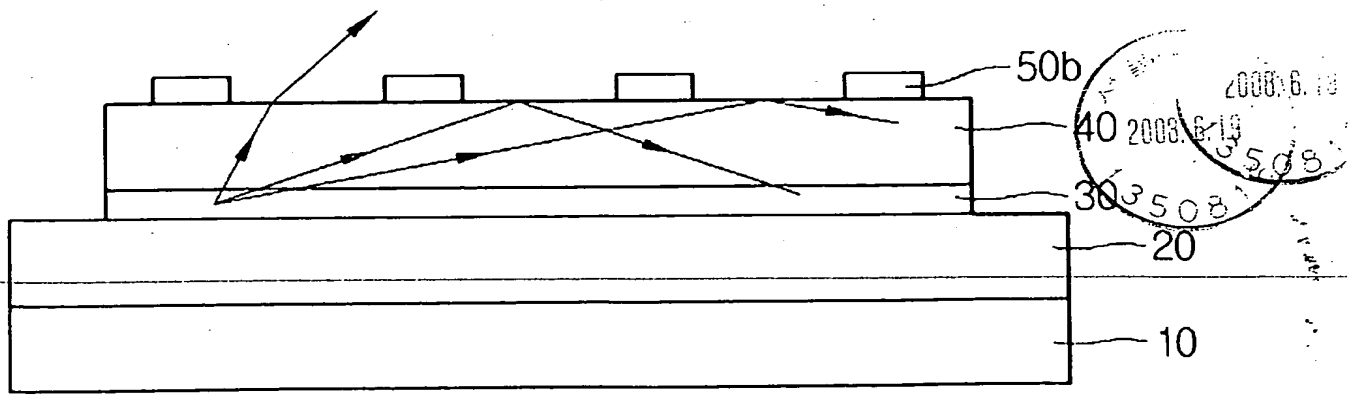
[Fig. 4]



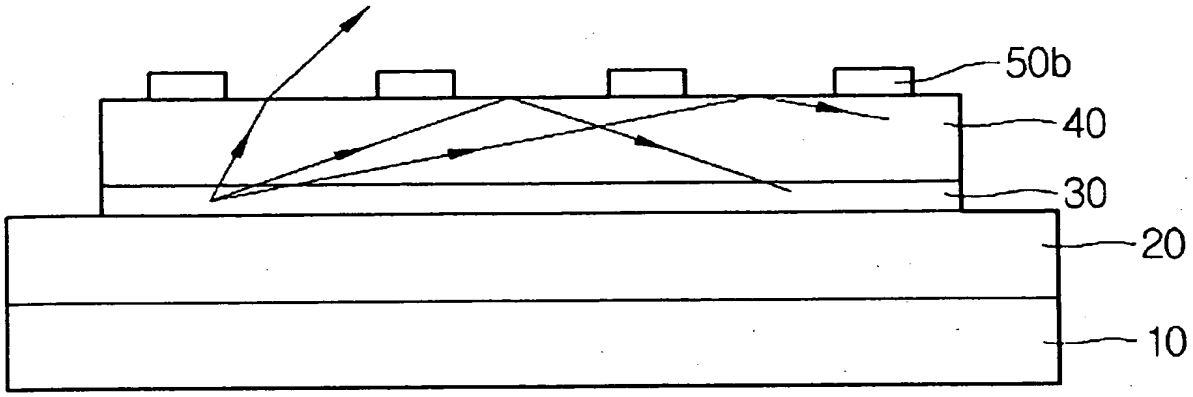
[Fig. 5]



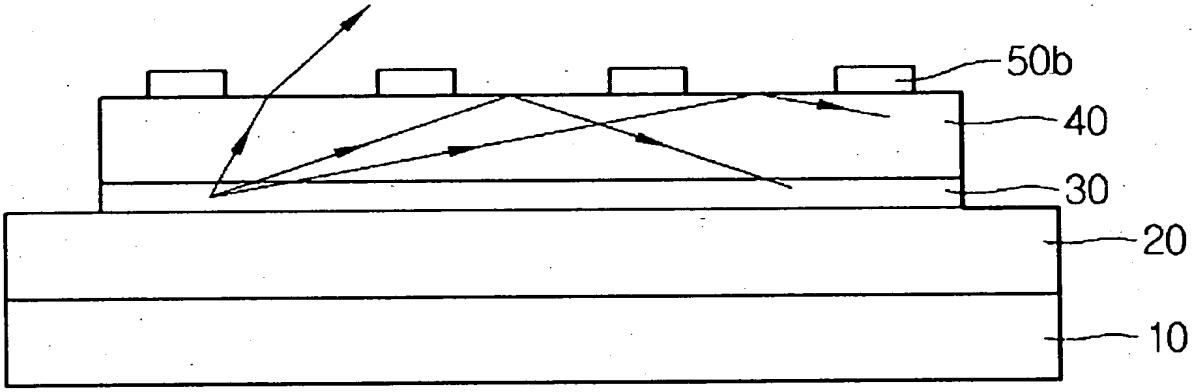
[Fig. 6]



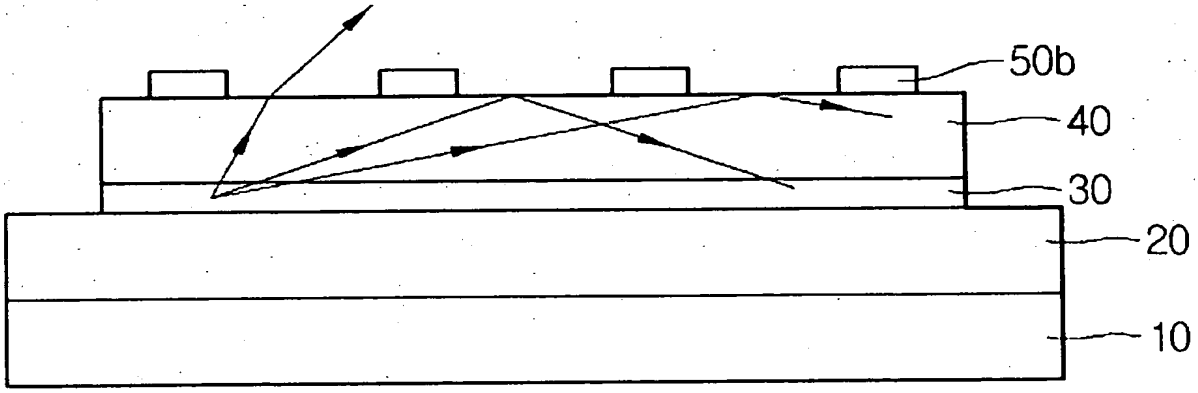
[Fig. 7]



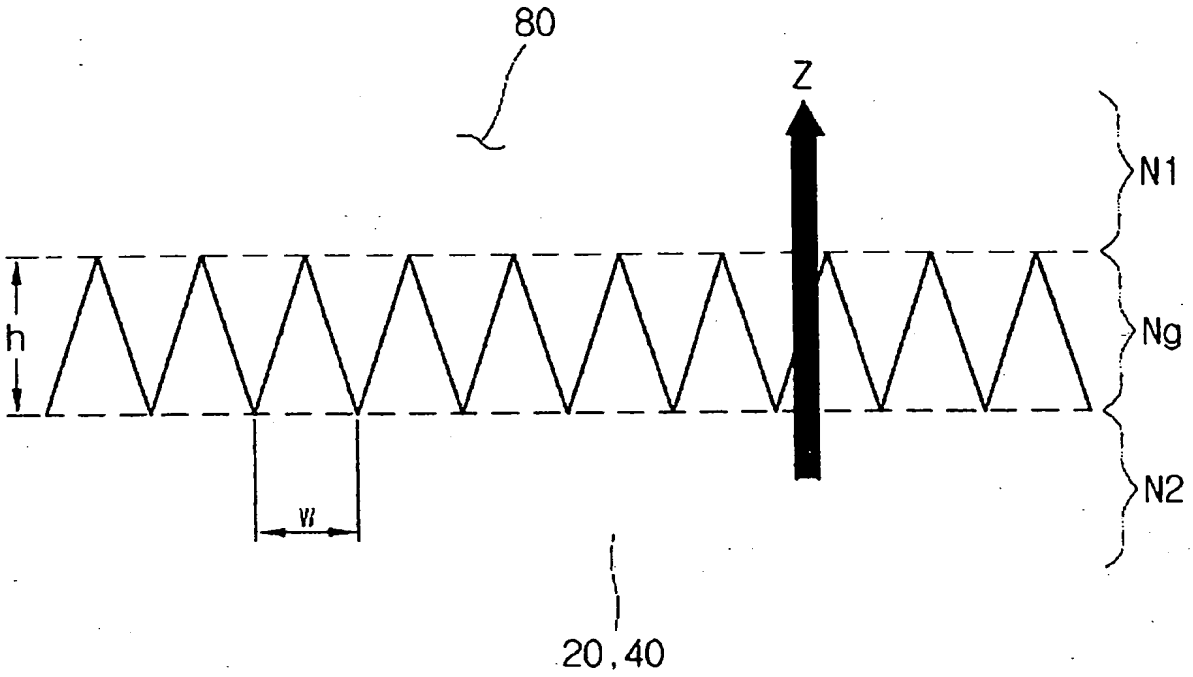
[Fig. 8]



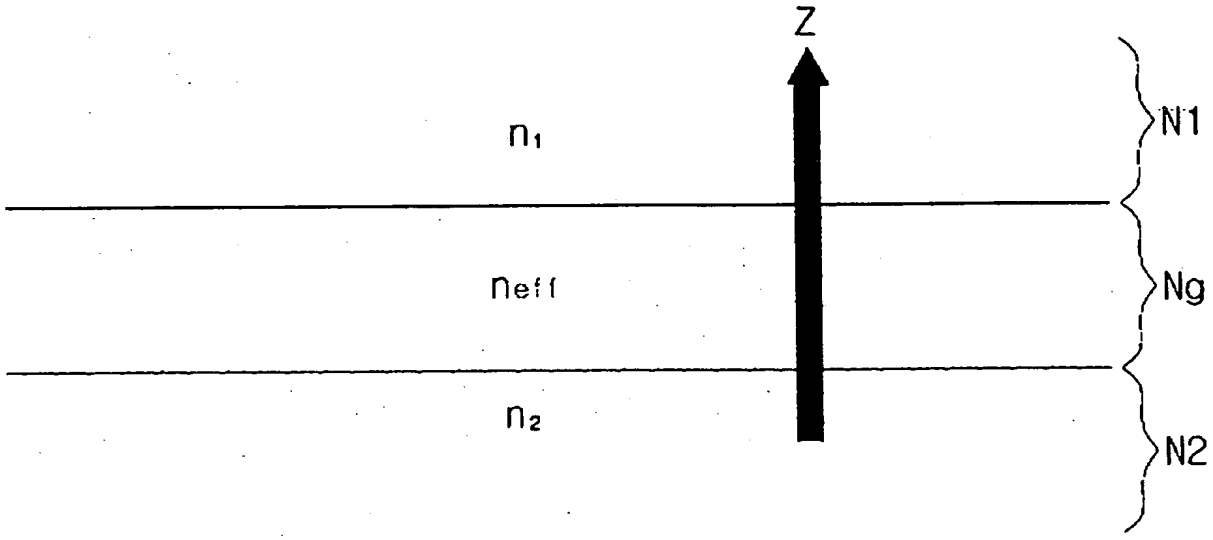
[Fig. 9]



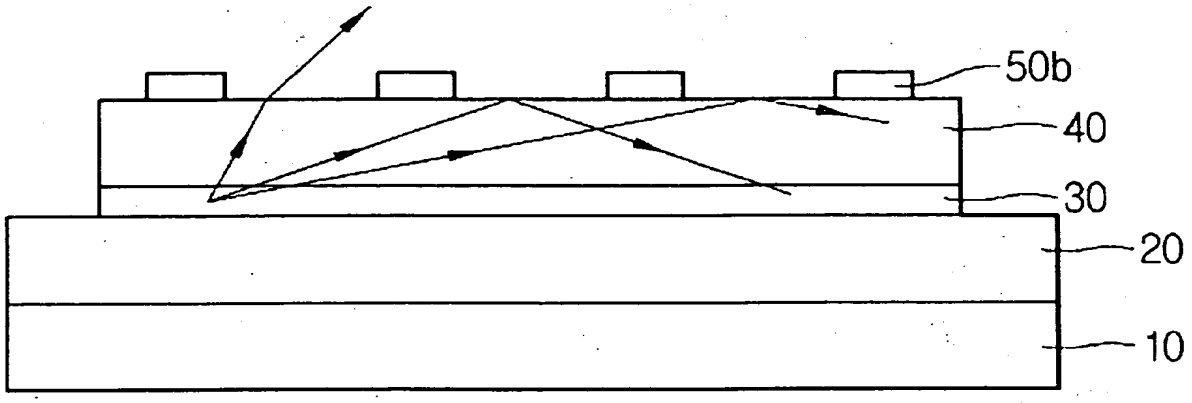
[Fig. 10]



[Fig. 11]



[Fig. 12]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2005/000036

A. CLASSIFICATION OF SUBJECT MATTER

IPC7 H01L 33/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L H01S

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean Patents and applications for inventions since 1975
Korean Utility models and applictions for Utility models since 1975
Japanese Utility models and application for Utility models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
e-KIPASS ; "LED", "REFLECT", "ELECTRODE", "UNEVEN", "ROUGH"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y A	US 2001/0048113 A1 (TAEK KIM) 6 DECEMBER 2001 see the abstract, figures 1-9, claim 1	1-6 7-16
Y A	US 6504180 B1 (IMEC VZW AND VRIJE UNIVERSITEIT) 7 JANUARY 2003 see the abstract, column 16 line 15 - line 37, figure 12	1-6 7-16
A	US 2003/0062530 A1 (KABUSHIKI KAISHA TOSHIBA) 3 APRIL 2003 see the abstract, paragraph [0087], claims 1-24, figures 1-9	1-16
E, Y E, A	KR 2005-0003671 A (EPIVALLEY CO., LTD.) 12 JANUARY 2005 see the abstract, figure 5	1-6 7-16

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 APRIL 2005 (15.04.2005)	**15 APRIL 2005 (15.04.2005)**

Name and mailing address of the ISA/KR	Authorized officer
Korean Intellectual Property Office 920 Dunsan-dong, Seo-gu, Daejeon 302-701, Republic of Korea Facsimile No. 82-42-472-7140	KIM, Dong Yup Telephone No. 82-42-481-5749

Form PCT/ISA/210 (second sheet) (January 2004)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/KR2005/000036

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2001/0048113 A1	06.12.2001	KR 1019980082472 A	05.12.1998
		US 64207358 B	16.07.2002
US 6504180 B1	07.01.2003	DE 69803519 T2	08.08.2002
		EP 00890830 A1	13.01.1999
		EP 00890830 B1	23.01.2002
		EP 00977063 A1	02.02.2000
		EP 00977064 A1	02.02.2000
		EP 00977277 A1	02.02.2000
		EP 00977280 A2	02.02.2000
		ES 2168703 T3	16.06.2002
		JP 11030559 A2	02.02.1999
		JP 12098180 A	07.04.2000
		JP 12106454 A	11.04.2000
		KR 1019990013488 A	25.02.1999
		US 2003075723 A1	24.04.2003
		US 63189018A	20.11.2001
		US 6623171 BB	23.09.2003
		US 6812161 BB	02.11.2004
		US 2002050561 AA	02.05.2002
		US 6186009 BA	13.02.2001
US 2003/0062530 A1	03.04.2003	JP 3469484 B2	25.11.2003
		JP 12196152 A	14.07.2000
		US 6495862 BA	17.12.2002
KR 2005-0003671 A	12.01.2005	WO 2005/004247 A1	13.01.2005

Attachment 8

KORYO INTERNATIONAL PATENT & LAW OFFICE

3rd Floor, 827-25 Yeoksam-dong, Gangnam-gu, Seoul

http://www.krparent.co.kr
E-mail: kr@krpatent.co.kr
Tel: 02-2186-8300
FAX: 02-2186-8301/2

2008-08-20

Recipient: **Choi, Pun-Jae** 203-1101 Hansol Apt., Songgang-dong, Yuseong-gu, Daejeon (KR)
Park, Jin-Soo 629 Beonji, Deongnim-ri, Jusan-myeon, Buan-gun, Jeollabuk-do (KR)
Sender: Koryo patent & law office Yeon-jung Kim(Administration), Se-Jun Oh(Technical)
Subject: Request for signing Declaration/Assignment forms. (For late submission)

---

1. Patent Registration Status

Country	U.S.	Type of Application	PCT National Phase Entry
Office Reference No.	XP16327-US		
Korean Application No.	P2004-18139	Korean Application Date	Mar 17, 2004
PCT International Application No.	PCT/KR2005/000036	PCT International Application Date	Jan 07, 2005
Local Attorney	HDP	Entry date	Sep 15, 2006
US Application No.	10/593,088		
Inventors	Choi, Pun-jae; Gong, Myeong-kook; Park, Jin-soo; CHOI, Hyeon Ryong; KIM, Seong Han		
Name of Invention	ANTI-REFLECTED HIGH EFFICIENCY LIGHT EMITTING DIODE DEVICE		

1. We note that the US national phase entry of above PCT/KR2005/000036 was completed on September 15, 2008. We enclose declaration and assignment forms for execution in order to complete formality of entering the US national phase. Please have the inventors sign and date in the documents, and return via Fax/E-mail before Aug 30, 2008.
2. Please refer to the enclosed Declaration/Assignment forms
3. If there are any inquiries, please contact the sender, Se-Jun Oh(technical) or Yeong-Jung Kim(administration) of Koryo Patent & Law Office.
   (Tel. 02-2186-8300, E-Mail: kr@krpatent.co.kr)

Koryo International Patent & Law Office

※Enclosed: 1. Application as filed

2. Declaration/Assignment Forms.

I hereby confirm that the concerned mail has been posted as a certification-of-content mail on Aug 20, 2008.
No. 3110513012244-3110513012245

Post Master,
Yeoksam-1-Dong Post Office, Seoul

고려국제특허법률사무소

서울시 강남구 역삼동 827-25 테라빌 3층

http:// www. krpatent.co.kr
E-maill : kr@krpatent.co.kr
TEL: 02-2186-8300
FAX : 02-2186-8301/2

2008 년 8 월 20 일

수 신 : 최번재(대전시 유성구 송강동 한솔아파트 203 동 1101 호
박진수(전라북도 부안군 주산면 덕림리 629 번지

발 신 : 고려특허법률사무소 오세준(기술)/김연정(관리) 발신대표 김연정

제 목 : 선언서/양도증 서명요청

---

1. 특허등록현황

국가	미 국	출원종류	PCT 국내단계진입
당소참조번호	XP16327-US		
우선권번호	P2004-18139	국내출원일	2004.3.17
PCT 출원번호	PCT/KR2005/000036	PCT 출원일	2005.01.07
현지 대리인	HDP	국내단계진입일	2006.09.15
미국출원번호	10/593,088		
발 명 자	최번재, 박진수, 김성한, 공명국, 조현룡		
발명 명칭	무반사 처리된 고효율 발광다이오드소자		
선언서/양도증 요청일	2008 년 8 월 30 일		

1. 상기 PCT출원 PCT/KR2005/000036의 2006년 9월 15일자로 미국 국내단계 진입이 완료된 본 건의 선언서/양도증 양식을 송부하오니, 발명자 서명과 날짜 기재하셔서 **2008년 8월 30일**까지 당소로 원본(팩스/이메일 가능)을 회송하여 주시기 바랍니다.

2. 본건의 출원서와 선언서/양도증 양식 동봉합니다.

3. 기타 위의 건에 대한 문의사항이 있으시면 기술담당자(오세준) 또는 관리담당자(김연정)앞으로 연락 주시기 바랍니다.

(Tel.02-2186-8314, E-maill:kr@krpatent.co.kr)

고려국제특허법률사무소

※ 첨부서류: 1. 출원서
2. 선언서/양도증

이 우편물은 2008-08-20
제 3110513012244-3110513012245호로
내용증명우편물로 발송하였음을 증명함
서울역삼1동우체국장

ASSIGNMENT

Atty. Docket No. **8947-000222/US**

WHEREAS, the undersigned, hereinafter referred to collectively as Assignor, has invented:

ANTI-REFLECTED HIGH EFFICIENCY LIGHT EMITTING DIODE DEVICE

for which Assignor is about to make or has made United States or International application for patent

(a) ☐ executed on even date preparatory to filing (each inventor should sign this Assignment on the same day as he/she signs the Declaration and Power of Attorney);

(b) ☐ executed on _____, _____, _____; or

(c) ☒ filed on January 7, 2005, and assigned Serial No. __ or PCT International Application No. PC/KR2005/000036; and

WHEREAS, EPIPLUS CO., LTD., Eyon-Hansan Industrial Park, 1027 Yulbuk-Ri, Chungbuk-Myun, Pyongtaek, Gyeonggi-do 451-833, Republic of Korea, hereinafter referred to as Assignee, is desirous of acquiring all right, title, and interest therein:

NOW, THEREFORE, for good and valuable consideration, the receipt and adequacy whereof is hereby acknowledged, Assignor agrees to, and hereby does, sell, assign and transfer unto Assignee and its successors in interest, the full and exclusive right, title and interest in the United States of America and throughout the world, including the right to claim priority under the laws of the United States, the Paris Convention, and any foreign countries, to the invention as described in the aforesaid application and all United States Letters Patent which may be granted therefore, and all divisions, continuations, reissues, reexaminations and extensions thereof, these rights, title and interest to be held and enjoyed by Assignee to the full end of the term for which the Letters Patent are granted and any extensions thereof as fully and entirely as the same would have been held by Assignor had this assignment and sale not been made, and the right to sue for, and recover for past infringements of, or liabilities for, any of the rights relating to any of the applications or patents resulting therefrom;

Assignor hereby covenants and agrees to execute all instruments or documents required or requested for the making and prosecution of any applications of any type for patent in the United States and in all foreign countries including, but not limited to, any provisional, continuation, continuation-in-part, divisional, renewal or substitute thereof, and as to letters patent any reissue, re-examination, or extension thereof, and for litigation regarding, or for the purpose of protecting title and to the said invention, the United States application for patent, or Letters Patent therefor, and to testify in support thereof, for the benefit of Assignee without further or other compensation than that above set forth;

Assignor hereby covenants that no assignment, sale, license, agreement or encumbrance has been or will be entered into which would conflict with this Assignment; and

Assignor hereby requests the United States Patent and Trademark Office to issue the Letters Patent of the United States of America to Assignee, and requests that any official of any country or countries foreign to the United States, whose duty it is to issue or grant patents and applications as aforesaid, to issue the Letters Patent, Utility Model Registration or Inventor's Certificate to Assignee.

The undersigned hereby grant(s) the law firm of Harness, Dickey & Pierce, P.L.C. the power to insert on this Assignment any further identification which may be necessary or desirable in order to comply with the rules of the U.S. Patent and Trademark Office for recordation of this document.

ASSIGNMENT

Atty. Docket No. **8947-000222/US**

_____

Pun Jae CHOI

_____

Dated

_____

Jin Soo PARK

_____

Dated

_____

Seong Han KIM

_____

Dated

_____

Myeong Kook GONG

_____

Dated

_____

Hyeon Ryong CHOI

_____

Dated

Atty. Dkt. No.: 8947-000222/US

DECLARATION AND POWER OF ATTORNEY (POA)

As a below named inventor, I hereby declare that:

My residence, mailing address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

ANTI-REFLECTED HIGH EFFICIENCY LIGHT EMITTING DIODE DEVICE

the specification of which (check one)

☐ is attached hereto.
or
☒ was filed on January 7, 2005 as Application Serial No. ____ or PCT International Application No. and was amended on PCT/KR2005/000036 (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. §§ 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or any PCT international application having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)				
APPN. SERIAL NO.	COUNTRY	DATE FILED (MM/DD/YYYY)	PRIORITY CLAIM Yes	PRIORITY CLAIM No
10-2004-0018139	KOREA	March 17, 2004	☒	☐
			☐	☐
			☐	☐

Atty. Dkt. No.: 8947-000222/US

DEC. AND POA Cont'd

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

PRIOR PROVISIONAL APPLICATION(S)	
APPN. SERIAL NO.	DATE FILED (MM/DD/YYYY)

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) listed below:

PRIOR U.S. APPLICATION(S)		
APPN. SERIAL NO.	DATE FILED (MM/DD/YYYY)	STATUS - PATENTED, PENDING, ABANDONED

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY

I hereby appoint the following attorneys with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

Thomas S. Auchterlonie	Reg. No. 37,275
John A. Castellano	Reg. No. 35,094
Terry L. Clark	Reg. No. 32,644
Donald J. Daley	Reg. No. 34,313
Gary D. Yacura	Reg. No. 35,416

and all individuals assigned to Customer No. **30593**.

Atty. Dkt. No.: 6947-000222/US

DEC. AND POA Cont'd

CORRESPONDENCE ADDRESS

I request the Patent and Trademark Office to direct all correspondence and telephone calls relative to this application to Harness, Dickey & Pierce, P.L.C., Customer No. 30593, P.O. Box 8910, Reston, Virginia, 20195, (703) 668-8000.

Full name of sole or first inventor: Pun-Jae CHOI

Inventor's signature: _____

Date: _____

Residence: 203-1101 Hansol Apt., Songgang-dong, Yuseong-gu, Daejeon KOREA

Citizenship: Republic of Korea

Mailing Address: Same as above

Full name of second joint inventor: Jin-Soo PARK

Inventor's signature: _____

Date: _____

Residence: 629 Beonji, Deongnim-ri, Jusan-myeon, Buan-gun, Jeollabuk-do, KOREA

Citizenship: Republic of Korea

Mailing Address: Same as above

Full name of third joint inventor: Seong-Han KIM

Inventor's signature: _____

Date: _____

Residence: 204-303 Hansol Apt., Songgang-dong, Yuseong-gu, Daejeon, KOREA

Citizenship: Republic of Korea

Mailing Address: Same as above

Atty. Dkt. No.: 8947-000222/US

DEC. AND POA Cont'd

Full name of fourth joint inventor: Myeong-Kook GONG

Inventor's signature: _____

Date: _____

Residence: 901-2003 LG-XI Apt., 869 Beonji, Sanghyeon-dong, Yongin, Gyeonggi-do KOREA

Citizenship: Republic of Korea

Mailing Address: Same as above

Full name of fifth joint inventor: Hyeon-Ryong CHOI

Inventor's signature: _____

Date: _____

Residence: 523-908 5 Danji Jugong Apt., Maetan 1-dong, Paldal-gu, Suwon, Gyeonggi-do KOREA

Citizenship: Republic of Korea

Mailing Address: Same as above

HARNESS DICKEY

John Castellano
Direct Dial: 703-668-8029
jcastellano@hdp.com

CONFIDENTIAL AND PRIVILEGED COMMUNICATION OF COUNSEL

September 15, 2006

VIA FACSIMILE & AIRMAIL
011-82-2-2186-8301

Mr. Hyuk-Soo Kwon
KORYO INTERNATIONAL PATENT & LAW OFFICE
SL. Kang Nam
P.O. Box 1132
Seoul 135-611
REPUBLIC OF KOREA

Re: Inventor(s): Pun Jae CHOI et al. – ***Filed: September 15, 2006***
Title: "ANTI-REFLECTED HIGH EFFICIENCY LIGHT EMITTING DIODE DEVICE"
Your Ref.: XP16327-US - Our Ref.: 8947-000222/US

Dear Mr. Kwon:

Further to your letter of September 14, 2006, this is to advise you that we filed the above-identified U.S. National Phase application on even date herewith in the U.S. Patent and Trademark Office. Enclosed herewith are copies of these papers as filed for your information and records. The items filed with the U.S. Patent and Trademark Office are as follows:

PCT Transmittal
Preliminary Amendment (6 pages)
Information Disclosure Statement
PTO-1449 Form w/ Listing Four (4) References, Enclosing One (1)
ISR, IPER
International Application as Filed
Formal Drawings (5 sheets)

Preliminary Amendment

We prepared and filed a Preliminary Amendment in connection with the present application to remove multiple dependent claims and to put the claims in better form for U.S. practice.

Further Information Requested

Since we filed the above-identified application without the declaration and assignment documents, please send us executed documents for filing with the U.S. Patent and Trademark Office as soon as possible as we expect to receive a Notice from the U.S.P.T.O. regarding these documents within the next two to five months.

In order to comply with the duty of disclosure, please provide us with copies of any relevant prior art cited in the specification (unless already provided) as well as any other prior art of which you are aware.

We shall forward the Official Filing Receipt, in due course and shall keep you advised of all further developments as they occur. If you have any questions, please do not hesitate to contact us.

Our Invoice for services rendered will follow with the confirmation copy of this letter.

Very truly yours,

HARNESS, DICKEY & PIERCE, P.L.C.

By_____
John A. Castellano

JAC:dpg

Enclosures: Copy of Papers as filed – One (1) copy
Updated Declaration (w/confirmation copy)
Updated Assignment (w/confirmation copy)
Two (2) Copies of Invoice

FORM PTO-1390 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE (Modified)

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	U.S. APPLICATION NO. (If known, see 37 CFR 1.5)	EXPRESS MAIL LABEL NO.
8947-000222/US	NEW	

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/KR2005/000036	January 7, 2005	March 17, 2004

TITLE OF INVENTION
ANTI-REFLECTED HIGH EFFICIENCY LIGHT EMITTING DIODE DEVICE

APPLICANT(S) FOR DO/EO/US
Pun Jae CHOI, Jin Soo PARK, Seong Han KIM, Myeong Kook GONG, and Hyeon Ryong CHO

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39 (1).
4. ☒ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is transmitted herewith.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4)
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3)).
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ An English language translation of the annexes of the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 20. below concern document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98-1449, International Search Report (PCT/ISA/210 and PCT/ISA/220) in English and PTO Form 1449
12. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. ☒ A FIRST preliminary amendment.
14. ☐ A SECOND or SUBSEQUENT preliminary amendment.
15. ☐ A substitute specification.
16. ☐ A change of power of attorney and/or address letter.
17. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821-1.825.
18. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
19. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
20. ☒ Other items or information: Formal Drawings; PCT/IB/337; PCT/ISA/237; PCT/IPEA/408; PCT/IPEA/409; PCT/RO/113

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U.S. APPLICATION NO (if known, see 37 CFR 1.5)	INTERNATIONAL APPLICATION NO	ATTORNEY'S DOCKET NUMBER
NEW	PCT/KR2005/000036	8947-000222/US

21. ☒ The following fees are submitted:

CALCULATIONS PTO USE ONLY

PCT FEES – NATIONAL STAGE:

Fee Code	Description	Fee
1631	Basic National Stage Fee	$300.00
1632	National Stage Search Fee	$400.00
1633	National Stage Examination Fee	$200.00

ENTER APPROPRIATE FEE AMOUNT =				$ 900.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☒ 30 Months from the earliest claimed priority date (37 CFR 1.492(e)).				$ 130.00	
PAGES	PAGES FILED	EXTRA PAGES FILED IN 50 PAGE SEGMENTS	RATE		
Total Pages	19 - 100 =0	0	X 250.00	$ 0.00	
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total Claims	16 - 20 =	0	X 50.00	$ 0.00	
Independent Claims	2 - 3 =	0	X 200.00	$ 0.00	
MULTIPLE DEPENDENT CLAIM(S) (if applicable)		____	+ 360.00	$ 0.00	
TOTAL OF ABOVE CALCULATIONS =				$ 1,030.00	
☐ Applicant claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.				$ ____	
SUBTOTAL =				$ 1,030.00	
Processing fee of $130.00 for furnishing the English translation later than ☐20 ☐30 Months from the earliest claimed priority date (37 CFR 1.492(f)).				$ ____	
TOTAL NATIONAL FEE =				$ 1,030.00	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). $40.00 per property +				$ ____	
TOTAL FEES ENCLOSED =				$ 1,030.00	
				Amount to be: refunded	$
				charged	$

a. ☒ A check in the amount of $1,030.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account. No. 08-0750 in the amount of $ to cover the above fees. A triplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 08-0750.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

Send all correspondence to:
Harness, Dickey & Pierce, P.L.C – Customer No. 30593
Post Office Box 8910
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Date: September 15, 2006

By _____
John A. Castellano, #35,094

JAC:dpg

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	NEW APPLICATION
International App. No.:	PCT/KR2005/000036
Filing Date:	September 15, 2006
Applicant:	Pun Jae CHOI et al.
Group Art Unit:	Unknown
Examiner:	Unknown
Title:	ANTI-REFLECTED HIGH EFFICIENCY LIGHT EMITTING DIODE DEVICE
Attorney Docket:	8947-000222/US

PRELIMINARY AMENDMENT

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

September 15, 2006

Sir:

The following preliminary amendments and remarks are respectfully submitted in connection with the above-identified application. Prior to examination of the present application, please consider the following:

Amendments to the Claims begin on page 2 of this Preliminary Amendment.

Remarks begin on page 5 of this Preliminary Amendment.

IN THE CLAIMS

This is a complete and current listing of the claims, marked with status identifiers in parentheses. The following listing of claims will replace all prior versions and listings of claims in the application.

Claims

1. (Previously Presented) A light emitting diode including a substrate, a N-type semiconductor layer, an active layer for generating light, and a P-type semiconductor layer, the light emitting diode comprising:

a first exposed region formed by etching the active layer and the P-type semiconductor layer to expose at least a part of the N-type semiconductor layer;

a first ohmic electrode formed on the first exposed layer;

a second ohmic electrode formed on the P-type semiconductor layer and having an opening at least a part of said P-type semiconductor layer having a second exposed region through said opening; and

said at least a part of P-type semiconductor layer being provided with an ultra-fine prominence and depression structure.

2. (Previously Presented) The light emitting diode as claimed in claim 1, wherein at least a part of the first exposed region excepting a portion having the first ohmic electrode has an ultra-fine prominence and depression structure.

3. (Previously Presented) A light emitting diode including a substrate, a N-type semiconductor layer, an active layer for generating light, a P-type semiconductor layer, a transparence metal (electrode), and a metal pad for wire bonding the light emitting diode comprising:

a first exposed region formed by etching the active layer and the P-type semiconductor layer to expose at least a part of the N-type semiconductor layer;

a first ohmic electrode formed on the first exposed layer; and

at least a part of said first exposed region excepting a portion having the first ohmic electrode being provided with an ultra-fine prominence and depression structure.

4. (Currently Amended) The light emitting diode as claimed in ~~any one of~~ claims 1~~—3~~, wherein the P-type semiconductor layer is GaN doped with Mg the N-type semiconductor layer is GaN doped with Si, and the active layer is GaN.

5. (Currently Amended) The light emitting diode as claimed in ~~any one of~~ claims 1~~—3~~, wherein the ultra-fine prominence and depression structure is a cluster of cylinder type prominence and depression elements.

6. (Previously Presented) The light emitting diode as claimed in claim 5, wherein the cylinder type prominence and depression element is a cone type, a column type, or a column type having a depressed upper end.

7. (Previously Presented) The light emitting diode as claimed in claim 5, wherein a width of the cylinder type prominence and depression element is 0.005 ~ 3 μm , and a height is 0.1 ~ 1 μm.

8 (Previously Presented) The light emitting diode as claimed in claim 5, wherein a width of the cylinder type prominence and depression element is 0.01 ~ 0.5 μm , and a height is 0.2 ~ 0.7 μm.

9. (Previously Presented) The light emitting diode as claimed in claim 5, wherein a width of the cylinder type prominence and depression element is 0.01 ~ 2 times larger than a peak wavelength of the light emitting diode, and a height is 0.5 ~ 10 times larger than the peak

wavelength.

10. (Previously Presented) The light emitting diode as claimed in claim 5, wherein a width of the cylinder type prominence and depression element is 0.1 ~ 1 times larger than a peak wavelength of the light emitting diode, and a height is 1 ~ 3 times larger than the peak wavelength.

11. (Previously Presented) The light emitting diode as claimed in claim 5, wherein a density of the cylinder type prominence and depression elements is 1 ~ 10000/ μm^2.

12. (Previously Presented) The light emitting diode as claimed in claim 5, wherein a density of the cylinder type prominence and depression elements is 50 ~ 500/ μm^2.

13. (Previously Presented) The light emitting diode as claimed in claim 5, wherein the cylinder type prominence and depression element is formed by depositing a metal or silicon compound on the semiconductor layer, heat-treating the deposited metal or silicon compound, and dry- or wet-etching the deposited metal or silicon compound.

14. (Previously Presented) The light emitting diode as claimed in claim 13, wherein the metal is any one or combinations selected from a group of Ag Al, Au, Cr, In, Ni, Pd, Pt and Ti.

15. (Previously Presented) The light emitting diode as claimed in claim 13, wherein a temperature for the heat-treating is ranged from 90 °C to 400 °C.

16. (Previously Presented) The light emitting diode as claimed in claim 15, wherein the cylinder type prominence and depression element is formed by selectivity, said selectivity being partly changed due to a reaction of the metal and the semiconductor at time of etching.

REMARKS

It should be noted that the amendments to original claims 1-16 of the present application are non-narrowing amendments, made solely to place the claims in proper form for U.S. practice and not to overcome any prior art or for any other statutory considerations. Other amended claims have been made to broaden the claims; remove multiple dependencies in the claims; remove/change any phrases unique to European practice; and to place claims in a more recognizable U.S. form. Other such non-narrowing amendments include placing apparatus-type claims (setting forth elements in separate paragraphs) in a more recognizable U.S. form. Again, all amendments are non-narrowing and have been made solely to place the claims in proper form for U.S. practice and not to overcome any prior art or for any other statutory considerations.

CONCLUSION

Accordingly, in view of the above amendments and remarks, an early indication of the allowability of each of claims 1-16 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY & PIERCE, P.L.C

By: _____
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PATENT
8947-000222/US

IN THE U.S. PATENT AND TRADEMARK OFFICE

Applicant(s):	Pun Jae CHOI et al.
Int'l Application No.:	PCT/KR2005/000036
Application No.:	NEW
Filed:	September 15, 2006
For:	ANTI-REFLECTED HIGH EFFICIENCY LIGHT EMITTING DIODE DEVICE

INFORMATION DISCLOSURE STATEMENT (SUBMISSION CONCURRENT WITH THE FILING OF A NEW PATENT APPLICATION)

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314
Mail Stop PCT

September 15, 2006

Sir:

Pursuant to 37 C.F.R. §§ 1.97 and 1.98, applicant(s) hereby submit(s) an Information Disclosure Statement for consideration by the Examiner.

I. LIST OF PATENTS, PUBLICATIONS OR OTHER INFORMATION

The patents, publications, or other information submitted for consideration by the Office are listed on PTO-1449, attached hereto.

II. COPIES

☐ Submitted herewith is a legible copy of (i) each U.S. and foreign patent; (ii) each publication or that portion which caused it to be listed; and (iii) all other information or that portion which caused it to be listed.

☒ This application is a National Phase of a PCT application. Some or all of the documents listed on the PTO-1449 are not enclosed because they were cited in the International Search Report and copies should be forwarded from the International Search Authority. If copies are needed, please contact the undersigned.

☐ Because the present application is being filed after June 30, 2003, no copies of the U.S. patents or U.S. patent application publications which are listed on the attached Form 1449 are enclosed pursuant to the waiver of 37 C.F.R. § 1.98(a)(2)(i). Any foreign patent documents or non-patent literature listed on the attached Form 1449 are enclosed herewith.

III. CONCISE EXPLANATION OF THE RELEVANCE
(check at least one box)

a. ☐ **DOCUMENTS IN THE ENGLISH LANGUAGE**

Some of the attached patents, publications, or other information in the English language do not require a statement of relevancy.

b. ☒ **DOCUMENTS NOT IN THE ENGLISH LANGUAGE**

A concise explanation of the relevance of all patents, publications, or other information listed that is not in the English language is as follows:

Many of the documents have been discussed in the PCT Search Report, the PCT Preliminary Examination Report, and/or throughout the specification. The PCT Search Report and PCT Preliminary Examination Report, along with a German translation aid translating key terms into English, indicate the degree of relevance found by the PCT Office, thereby satisfying the requirement for a concise explanation. See MPEP 609(A)(3).

c. ☒ **ENGLISH LANGUAGE SEARCH REPORT**

An English language version of the search report or action that indicates the degree of relevance found by the foreign office is attached, thereby satisfying the requirement for a concise explanation. See MPEP 609(A)(3).

d. ☐ **OTHER**

The following additional information is provided for the Examiner's consideration.

e. ☐ **EQUIVALENCY DOCUMENTS**

FEES

This Information Disclosure Statement is being filed concurrently with the filing of a new patent application; therefore, no fee is required.

If the Examiner has any questions concerning this IDS, he/she is requested to contact the undersigned. If it is determined that this IDS has been filed under the wrong rule, the PTO is requested to consider this IDS under the proper rule and charge the appropriate fee to Deposit Account No. 08-0750.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY & PIERCE, P.L.C.

By: _____
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Enclosures:

- ☒ Form PTO-1449(s)
- ☒ Documents
- ☒ International Search Report (PCT/ISA/210 and PCT/ISA/220)
- ☒ International Preliminary Examination Report (PCT/IPEA/416 and PCT/IPEA/409)
- ☐ Fee

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Form PTO-1449	ATTY DOCKET NO. 8947-000222/US	APPLICATION NO. NEW
INFORMATION DISCLOSURE CITATION IN AN APPLICATION (Use several sheets if necessary)	APPLICANTS Pun Jae CHOI et al.	CONF. NO. Unknown
	FILING DATE September 15, 2006	GROUP Unknown

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	US 2001/0048113 A1	12/6/2001	Kim			
	US 6,504,180 B1	1/7/2003	Heremans			
	US 2003/0062530 A1	4/3/2003	Toshiba			

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES	TRANSLATION NO
	KR 2005-0003671 A	1/12/2005	KOREA				

OTHER DOCUMENTS

(Include Name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

JAC:dpg

Description

ANTI-REFLECTED HIGH EFFICIENCY LIGHT EMITTING DIODE DEVICE

Technical Field

[1] The present invention relates to a light emitting diode, and in particular, relates to an anti-reflected light emitting diode having an ultra-fine prominence and depression to increase a light extraction efficiency.

Background Art

[2] Generally, a light emitting diode(hereafter referred as 'LED') is a kind of solid-state device for converting an electric energy to light, and have two semiconductor layers(N-type, and P-type) oppositely doped with each other and an active layer positioned between the layers. When a bias is applied to the two semiconductor layers, holes and electrons are injected into the active layer to be recombined to generate light. The light generated in the active region is omnidirectionally emitted, and a part of the light is emitted to the outside of semiconductor chip through a surface exposed to the outside.

[3] Recently, as the material for semiconductor is improved, the efficiency of semiconductor chip is also increased. New type LED is made of GaN group material to permit an efficient illumination in a spectrum from ultraviolet ray to green ray. As the LED is improved, the LED is expected to substitute prior art lighting used in a traffic signal lamp, an indoor or outdoor display, a headlight and a tail-light for vehicle, and prior art indoor lighting device. However, the prior art LED cannot emit all the light generated in the active layer. Thus, the efficiency is restricted.

[4] Fig. 1 is a cross-sectional view of prior art light emitting diode provided with a mesh-type ohmic contact. After a N-type semiconductor layer 20, an active layer 30, and a P-type semiconductor layer 40 are in sequence deposited on a substrate 10, a mesh-type ohmic contact 50b is formed. The mesh-type is a structure having openings through which a part of the N-type semiconductor layer 40 is exposed. If, the ohmic electrode 50b having openings is not formed on the P-type semiconductor layer and, instead, a transparence metal(PT) is formed on the layer, a part of light generated in the active layer 30 is reflected at the P-type semiconductor layer 40 and the transparence metal. Even though a part of light is passed through the transparence metal, as the light is a degree of 400 nm of visual ray, a boundary condition is not satisfied in the thin transparence metal having a thickness of a few nm ~ several tens

nm to occur a loss of light. Therefore, by applying the ohmic electrode 50b having the openings, the light generated in the active layer is passed to the air through the openings, or through the openings and an epoxy resin to reduce the loss of light.

[5] The LED provided with the ohmic electrode 50b has a problem. The typical refractive index of semiconductor material is about 2.2 ~ 3.8, which is higher than that of the air(n=1.0) and encapsulating epoxy(n ≒ 1.5). According to Snell's law, a light, with an angle larger than a critical angel, moved from a region with high refractive index to a region with low refractive index is not passed to the outside and is totally reflected to the inside(that is, Total Internal Reflection : TIR). Therefore, a part of light emitted from the active layer 30 cannot be passed through a surface, in contact with the air or the epoxy, of the P-type semiconductor layer 40 and is totally reflected to the inside at the surface. The reflected light continues reflections until absorbed in the LED, or is emitted to the outside through other surfaces. Thus, there is a problem that a light extraction efficiency is lowed in the light emitting diode with the mesh-type ohmic electrode.

Disclosure of Invention

Technical Solution

[6] Therefore, an object of the present invention is to solve the problems involved in the prior art, and to provide a light emitting diode in which a light generated is not reflected from a semiconductor layer having an ultra-fine prominence and depression structure and is emitted to the outside to increase a light extraction efficiency.

[7] According to one embodiment of the present invention, in a light emitting diode having a substrate, a N-type semiconductor layer, an active layer for generating light and a P-type semiconductor layer, the light emitting diode further comprises: a first exposed region formed by etching the active layer and the P-type semiconductor layer to partly expose the N-type semiconductor layer; a first ohmic electrode formed on the first exposed region; and a second ohmic electrode formed on the P-type semiconductor layer, and having an opening to partly form a second exposed region on the P-type semiconductor layer. At least a part of the second exposed region is formed to have an ultra-fine prominence and depression.

[8] Preferably, at least a part of the first exposed region excepting a portion having the first ohmic electrode has a prominence and depression structure.

[9] According to other embodiment of the present invention, in a light emitting diode having a substrate, a N-type semiconductor layer, an active layer for generating light, a P-type semiconductor layer, a transparence metal(electrode), and a metal pad for wire

bonding the light emitting diode further comprises: a first exposed region formed by etching the active layer and the P-type semiconductor layer to expose at least a part of the N-type semiconductor layer; and a first ohmic electrode formed on the first exposed region. At least a part of the first exposed region excepting a portion having the first ohmic electrode is formed to have an ultra-fine prominence and depression.

[10] In the embodiments, the P-type semiconductor layer is preferably GaN doped with Mg, the N-type semiconductor layer is preferably GaN doped with Si, and the active layer is preferably GaN.

[11] In the embodiments, the ultra-fine prominence and depression is preferably a cluster of a cylinder shaped prominence and depression elements.

[12] In the embodiments, the cylinder shaped prominence and depression element is substantially a cone type, a column type, or a cylinder having the depressed upper end.

[13] In the embodiments, the width of the prominence and depression element is preferably 0.005 ~ 3μm, and more preferably 0.01 ~ 0.5μm. The height of the prominence and depression element is preferably 0.1 ~ 1μm, and more preferably 0.2 ~ 0.7μm.

[14] In the embodiments, the width of the prominence and depression element is 0.01 ~ 2 times larger than a peak wavelength of light emitted from the light emitting diode, and more preferably 0.1 ~ 1 times larger. The height of the prominence and depression element is 0.5 ~ 10 times larger than the peak wavelength of light emitted from the light emitting diode, and more preferably 1 ~ 3 times larger.

[15] In the embodiments, the density of the prominence and depression elements is preferably 1 ~ 10000/μm^2, and more preferably 50 ~ 500/μm^2.

[16] According to the embodiments, the light extraction efficiency can be increased.

Description of Drawings

[17] The above objects, other features and advantages of the present invention will become more apparent by describing the preferred embodiment thereof with reference to the accompanying drawings, in which:

[18] Fig. 1 is a cross-sectional view of prior art light emitting diode provided with a mesh-type ohmic contact;

[19] Fig. 2 is a schematic perspective view of a light emitting diode according to one embodiment of the present invention;

[20] Fig. 3 is a cross-sectional view taken along line S1 in Fig. 2;

[21] Fig.4 is a cross-sectional view of a light emitting diode according to other embodiment of the present invention;

[22] Fig. 5 is a diagram showing various examples of a discrete prominence and depression element used in an ultra-fine prominence and depression structure formed on a light emitting diode according to the present invention;

[23] Fig. 6 is an enlarged picture showing an ultra-fine prominence and depression structure of high density;

[24] Fig. 7 is an enlarged picture showing an ultra-fine prominence and depression structure of low density;

[25] Fig. 8 is an enlarged picture showing a thick ultra-fine prominence and depression structure;

[26] Fig. 9 is an enlarged picture showing thin ultra-fine prominence and depression structure;

[27] Fig. 10 and 11 are schematic diagrams showing an ultra-fine prominence and depression structure formed on a light emitting diode according to the present invention; and

[28] Fig. 12 is a graph illustrating the characteristic of optical power of a light emitting diode according to the present invention.

[29] *Brief Description of reference number*

[30] 10: light-permeable sapphire substrate A1: first exposed region

[31] 20: N-type semiconductor layer A2: second exposed region

[32] 30: active layer 60: transparence metal

[33] 40: P-type semiconductor layer 70: metal pad for wire bonding

[34] 50a: first ohmic electrode 80: air

[35] 50b: second ohmic electrode

Best Mode

[36] Reference will now be made in detail to an anti-reflected high efficiency light emitting diode device according to the present invention by using the accompanying drawings. In the following explanation, a description through accompanying drawings will be added in order to facilitate further complete understanding of the present invention, but it is apparent to those skilled in the art that the present invention can be carried out without a detailed description of the drawings. In cases, a description of the main elements or constituents of the known technology will be omitted if it obscures the point of the present invention unnecessarily. This is intended to avoid any possibility to obscure the description of the present invention.

[37] Fig. 2 is a schematic perspective view of a light emitting diode according to one embodiment of the present invention, and Fig. 3 is a cross-sectional view taken along

line S1 in Fig. 2.

[38] With reference to Fig. 2 and Fig. 3, in order to realize the present invention, a N-type semiconductor layer 20, an active layer 30 and a P-type semiconductor 40 are in sequence formed on a substrate 10 by using an epitaxial process. The substrate 10 can be a light-permeable sapphire substrate. The N-type semiconductor layer 20 is formed by GaN(Gallium Nitride) doped with Si, but not restricted to the same. The P-type semiconductor layer 40 is formed by GaN doped with Mg, but not restricted to the same. The active layer 30 formed by one selected from GaN, AlGaN and InGaN, and the amount of the Al and the In can be adjusted according to a kind of light generated in the active layer.

[39] Next, a part of the active layer 30 and the P-type semiconductor layer 40 is etched by using a photo lithography process to expose the N-type semiconductor layer 20. Then, a first exposed region A1 is formed on the N-type semiconductor layer 20. Preferably, the first exposed region A1 is formed on the margin portions of the N-type semiconductor layer 20 by etching the edge portions of the active layer 30 and P-type semiconductor layer 40. Then, a first rectangular shaped ohmic electrode 50a is formed on one of the margin portions of the N-type semiconductor layer 20 by etching the active layer 30 and the P-type semiconductor layer 40.

[40] Next, an ultra-fine prominence and depression structure is formed on the first exposed region A1 excepting the portion having the first ohmic electrode 50a, and on a second exposed region A2. The reason why the ultra-fine prominence and depression structure is formed is to emit the light generated in the active layer 30 to outside without a reflection in the first exposed region A1 and the second exposed region A2. The structure of prominence and depression and method for forming the same will be described later with reference to Fig. 5 - Fig. 9. The second exposed region A2 is an exposed portion of the P-type semiconductor layer 40 excepting a portion having a second ohmic electrode 50b thereon. The exposed region includes portions exposed through openings of the second ohmic electrode 50b.

[41] After forming the prominence and depression on the N- and the P-type semiconductor layers, the first ohmic electrode 50a is formed on a part of the first exposed region A1, and the second ohmic electrode 50b is formed on the P-type semiconductor layer 40 through a photo lithography process.

[42] As the ultra-fine prominence and depression structure is not formed under the first ohmic electrode 50a and the second ohmic electrode 50b, the under surfaces of the first and the second ohmic electrodes 50a and 50b maintain smoothness. The material for

the ohmic electrodes 50a and 50b is selected from any one of Ti, Al, Au, Ni, Pt, Pd, Ag Rh or compound of the elements. If a white metal such as Al, Pt and Cr is used, the reflexibility of the under surfaces can be increased.

[43] In above description, the method for forming the ultra-fine prominence and depression structure on the N-type semiconductor layer 20 and the P-type semiconductor layer 40 excepting the portions having the ohmic electrodes 50a and 50b thereon before forming the ohmic electrodes 50a and 50b. However, the ultra-fine prominence and depression structure can be formed on the N-type semiconductor layer 20 and the P-type semiconductor layer 40 excepting the portions having the ohmic electrodes 50a and 50b thereon after forming the ohmic electrodes 50a and 50b. In this case, the ohmic electrodes function as a self-aligner.

[44] According to the embodiment, as the light generated in the active layer 30 is not reflected into the inside of the active layer by the ultra-fine prominence and depression structure which is formed on the first exposed region A1 excepting the portion having ohmic electrode 50a and on the second exposed regions A2, the light extraction efficiency of the light emitting diode is increased.

[45] Fig. 4 is a cross-sectional view of a light emitting diode according to other embodiment of the present invention. When comparing the light emitting diode in Fig. 4 with that of Fig. 3, a ultra-fine prominence and depression structure is not formed on the P-type semiconductor layer, and a light permeable electrode(transparence metal) 60 and a metal pad 70 for wire bonding are instead formed on the P-type semiconductor layer in Fig. 4. An ultra-fine prominence and depression structure is formed on the first exposed region A1 of the N-type semiconductor layer 20 excepting the portion having the ohmic electrode 50a as is in Fig. 3.

[46] According to the embodiment, the light generated in the active layer, which is projected into the P-type semiconductor layer 40 with an incidence angle larger than a critical angle, is totally reflected to the inside by the light permeable electrode 60, and to be projected into the N-type semiconductor layer 20. The light projected into the N-type semiconductor layer is reflected again at the bottom of the layer to be emitted to the outside of the layer through the exposed region A1 without a refection.

[47] Further, in the embodiment, as the first ohmic electrode 50a is formed to have a smooth bottom surface as is in Fig. 3, the light projected to the bottom surface is reflected to the inside and emitted to the outside to increase the light extraction efficiency.

[48] Fig. 5 is a diagram showing various example of a discrete prominence and

depression element used in an ultra-fine prominence and depression structure formed on a light emitting diode according to the present invention.

[49] The ultra-fine prominence and depression structure is a cluster of a cylinder shaped prominence and depression elements having a few ?(Angstrom) ~ a few nm(nano-meter) dimensions . Each of the prominence and depression elements has a different size and shape. The width(w) of the discrete prominence and depression element is about 0.005 ~ 3μm, and preferably 0.01 ~ 0.5μm. The height of the discrete prominence and depression element is about 0.1 ~ 1μm, and preferably 0.2 ~ 0.7μm.

[50] The dimension(width or height) of the prominence and depression element is similar to that of a peak wavelength(λp) of light generated in the light emitting diode. The width(w) of the prominence and depression element is 0.01 ~ 2 times larger than the peak wavelength of light, and preferably 0.1 ~ 1 times. The height of the prominence and depression element is 0.5 ~ 10 times larger than the peak wavelength of light, and preferably 1 ~ 3 times larger.

[51] As shown in Fig. 5, the discrete prominence and depression element has various shapes. The shape of the element is generally a cylinder type protruded from the semiconductor layers 20 and 40. More detail, the shape is similar to a cone or a column, or is a column having a depressed upper end. A small number of ruggedness ~ tens of thousands of ruggedness much smaller than the prominence and depression element can be formed on the depressed upper end.

[52] Fig. 6 ~ Fig. 9 are enlarged pictures showing a prominence and depression structure formed on a light emitting diode according to the present invention. Fig. 6 shows a prominence and depression structure of high density, Fig. 7 shows a prominence and depression structure of low density, Fig. 8 shows a thick prominence and depression structure, and Fig. 9 shows a thin prominence and depression structure.

[53] The term 'density' used in here means the number of the prominence and depression element per the unit area[unit/μm]. The term 'high density' means that numbers of ruggedness are densely formed. The density of the prominence and depression elements is about 1 ~ 10000/ μm^2, and more preferably 50 ~ 5000/μm^2.

[54] The term 'thick' means that the height(h) is smaller than the width(w).

[55] There are various methods for forming the prominence and depression structure on the semiconductor layers 20 and 40. In one method, a metal cluster is formed by depositing a metal(Ag, Al, Au, Cr, In, Ir, Ni, Pd, Pb, Pt, Rd, Sn, Ti, W, or a compound of the elements) on the first exposed region A1 of the N-type semiconductor layer 20 and on the P-type semiconductor layer 40 and heat-treating the metal in high

temperature. Next, the metal cluster in a portion to be formed with the first ohmic electrode 50a in the first exposed region and in a portion to be formed with the second ohmic electrode 50b in the P-type semiconductor layer 40 is removed by a photo lithography process. Next, the ultra-fine prominence and depression structure is formed by dry- or wet-etching the rest of metal cluster on the first exposed region A1 excepting the portion to be formed with the first ohmic electrode 50a and on the second exposed region A2.

[56] In other method, the prominence and depression structure is formed by etching the first exposed region A1 excepting the portion to be formed with the first ohmic electrode 50a, and the second exposed region A2 using ICP and RIE through a photo lithography process, after growing roughly a silicon compound such as SiO_2 and Si_3N_4 on the exposed regions by using a porous growing method.

[57] Further, after growing silicon compound such as SiO_2 and Si_3N_4, and forming a metal cluster by depositing a metal(Ag, Al, Au, Cr, In, Ir, Ni, Pd, Pb, Pt, Rd, Sn, Ti, W or a compound of elements) on the silicon compound and heat-treating the deposited metal in high temperature, the prominence and depression structure is formed by selectively (wet or dry)etching the metal cluster on the first exposed region A1 excepting the portion to be formed with the first ohmic electrode 50a, and the second exposed region A2 through a photo lithography process.

[58] The examples for forming the prominence and depression structure on the semiconductor layers 20 and 40 by using the methods are as follow.

[59] [Example 1] High Density, Thin type

[60] Type : Thin type (Width(w) : about 0.01 ~ 0.03μm/ Height(h):about 0.5μm)

[61] Density : about 40 ~ 70/μm^2

[62] Used Metal : Ni, Au(20? ~ 50?) (or In, Au and Ni compound used)

[63] Heat treating : 550 ℃ ~ 650 ℃ for 60sec ~ 120sec

[64] Dry etching : ICP treating for 300sec

[65] [Example 2] High Density, Thick type

[66] Type : Thick type (Width(w) : about 0.08 ~ 0.15μm/ Height(h):about 0.5μm)

[67] Density : about 40 ~ 70/μm^2

[68] Used Metal : Ni, Au(50? ~ 100?) (or In, Au and Ni compound used)

[69] Heat treating : 550 ℃ ~ 650 ℃ for 60sec ~ 120sec

[70] Dry etching : ICP treating for 300sec

[71] [Example 3] Low Density, Thin type

[72] Type : Thin type (Width(w) : about 0.01 ~ 0.03μm/ Height(h):about 0.5μm)

[73] Density : about 4 ~ 8/μm^2

[74] Used Metal : Ni, Au(20? ~ 50?) (or In, Au and Ni compound used)

[75] Heat treating : 500 ℃ ~ 600 ℃ for 20sec ~ 30sec

[76] Dry etching : ICP treating for 300sec

[77] [Example 1] High Density, Thin type, Low Height

[78] Type : Thin type (Width(w) : about 0.08 ~ 0.15μm/ Height(h):about 0.3μm)

[79] Density : about 40 ~ 70/μm^2

[80] Used Metal : Ni, Au(50? ~ 100?) (or In, Au and Ni compound used)

[81] Heat treating : 550 ℃ ~ 650 ℃ for 60sec ~ 120sec

[82] Dry etching : ICP treating for 300sec

[83] Fig. 10 and Fig. 11 are schematic diagrams showing an ultra-fine prominence and depression structure formed on a light emitting diode according to the present invention. With reference to Fig. 10a, there are three layers in the Fig. That is, a semiconductor layer N2, an ultra-fine prominence and depression structure layer Ng and air layer are in the Fig. The ultra-fine prominence and depression structure is formed on the semiconductor layers 20 and 40, and the surface of the prominence and depression structure is in contact with air. The surface can also be in contact with an epoxy resin.

[84] As described above, each of the prominence and depression elements making up the prominence and depression structure has a width of 0.01 ~ 0.5μm and a height of 0.2 ~ 0.7μm, which are about 0.1 ~ 1 times larger than the peak wavelength(p λ).

[85] If the dimensions(w, h) of the prominence and depression element making up the prominence and depression structure is made to have a value similar to a wavelength of light generated in the active layer, a refractive index n_{eff} of the ultra-fine prominence and depression structure is changed in linear from a refractive index n_2 of the semiconductor layer N2 to a refractive index n_1 of the air layer N2. The semiconductor layer N2, the ultra-fine prominence and depression layer Ng and the air layer N1 can be conceptually represented as in Fig. 11.

[86] As the refractive index is linearly changed along the arrow Z, discontinuity of refractive index, that is boundary, is not present. As the boundary is not present, TIR(Total Internal Reflection) phenomenon is not occurred at the boundary. In the result, as a reflection is not occurred in the ultra-fine prominence and depression layer Ng, the ultra-fine prominence and depression layer Ng functions a Anti-reflection layer.

[87] As the theoretical description for the light characteristic in case of a structure

smaller than the wavelength of light being in a medium plane is disclosed in 'The optical properties of artificial media structured at a subwavelength scale, Encyclopedia of Optical Engineering pp. 62-71, 2003', detailed description will be omitted.

[88] As the semiconductor layers 20 and 40 are treated to have the anti-reflection layer, all of light generated in the active layer is emitted from the semiconductor layers 20 and 40 to the outside to increase the light extraction efficiency.

[89] Fig. 12 is a graph illustrating the characteristic of optical power of the light emitting diode according to the present invention. As shown in Fig. 12, the optical power of the light emitting diode according to the present invention is much higher than that of prior art light emitting diode.

[90] The optical power is different from embodiment to embodiment. As the height of the prominence and depression element and the density increase, the effect of the anti reflection can be increased.

[91] While the present invention has been described and illustrated herein with reference to the preferred embodiments thereof, it will be apparent to those skilled in the art that various modifications and variations can be made therein without departing from the spirit and scope of the invention. Thus, it is intended that the present invention covers the modifications and variations of this invention that come within the scope of the appended claims and their equivalents.

Industrial Applicability

[92] According to another aspect of the present invention, as the light extraction efficiency and the light generating efficiency are increased, a light emitting diode with high brightness can be fabricated.

[93] According to other aspect of the present invention, a current supply can be smoothly done by employing a mesh-type ohmic contact having the opening to increase the light generating efficiency.

[94] According to another aspect of the present invention, as the light extraction efficiency and the light generating efficiency are increased, a light emitting diode with high brightness can be fabricated.

Claims

[1] 1. A light emitting diode including a substrate, a N-type semiconductor layer, an active layer for generating light, and a P-type semiconductor layer, the light emitting diode comprising:
a first exposed region formed by etching the active layer and the P-type semiconductor layer to expose at least a part of the N-type semiconductor layer;
a first ohmic electrode formed on the first exposed layer;
a second ohmic electrode formed on the P-type semiconductor layer and having an opening, at least a part of said P-type semiconductor layer having a second exposed region through said opening; and
said at least a part of P-type semiconductor layer being provided with an ultra-fine prominence and depression structure.

2. The light emitting diode as claimed in claim 1, wherein at least a part of the first exposed region excepting a portion having the first ohmic electrode has an ultra-fine prominence and depression structure.

3. A light emitting diode including a substrate, a N-type semiconductor layer, an active layer for generating light, a P-type semiconductor layer, a transparence metal(electrode), and a metal pad for wire bonding, the light emitting diode comprising:
a first exposed region formed by etching the active layer and the P-type semiconductor layer to expose at least a part of the N-type semiconductor layer;
a first ohmic electrode formed on the first exposed layer; and
at least a part of said first exposed region excepting a portion having the first ohmic electrode being provided with an ultra-fine prominence and depression structure.

4. The light emitting diode as claimed in any one of claims 1 - 3, wherein the P-type semiconductor layer is GaN doped with Mg, the N-type semiconductor layer is GaN doped with Si, and the active layer is GaN.

5. The light emitting diode as claimed in any one of claims 1 - 3, wherein the ultra-fine prominence and depression structure is a cluster of cylinder type prominence and depression elements.

6. The light emitting diode as claimed in claim 5, wherein the cylinder type prominence and depression element is a cone type, a column type, or a column type having a depressed upper end.

7. The light emitting diode as claimed in claim 5, wherein a width of the cylinder type prominence and depression element is 0.005 ~ 3 ㎛ , and a height is 0.1 ~ 1 ㎛ .

8 The light emitting diode as claimed in claim 5, wherein a width of the cylinder type prominence and depression element is 0.01 ~ 0.5 ㎛ , and a height is 0.2 ~ 0.7 ㎛ .

9. The light emitting diode as claimed in claim 5, wherein a width of the cylinder type prominence and depression element is 0.01 ~ 2 times larger than a peak wavelength of the light emitting diode, and a height is 0.5 ~ 10 times larger than the peak wavelength.

10. The light emitting diode as claimed in claim 5, wherein a width of the cylinder type prominence and depression element is 0.1 ~ 1 times larger than a peak wavelength of the light emitting diode, and a height is 1 ~ 3 times larger than the peak wavelength.

11. The light emitting diode as claimed in claim 5, wherein a density of the cylinder type prominence and depression elements is 1 ~ 10000/ μm^2 .

12. The light emitting diode as claimed in claim 5, wherein a density of the cylinder type prominence and depression elements is 50 ~ 500/ μm^2 .

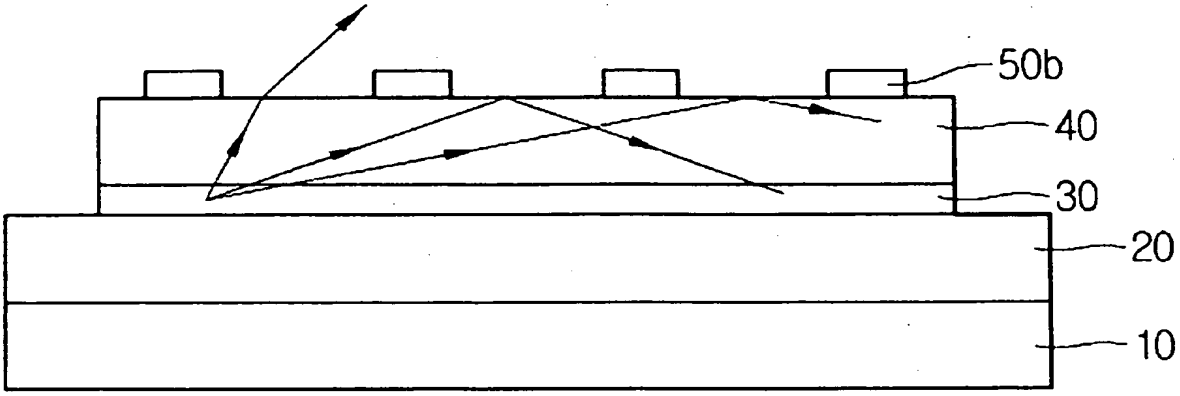
13. The light emitting diode as claimed in claim 5, wherein the cylinder type prominence and depression element is formed by depositing a metal or silicon compound on the semiconductor layer, heat-treating the deposited metal or silicon compound, and dry- or wet-etching the deposited metal or silicon compound.

14. The light emitting diode as claimed in claim 13, wherein the metal is any one or combinations selected from a group of Ag, Al, Au, Cr, In, Ni, Pd, Pt and Ti.

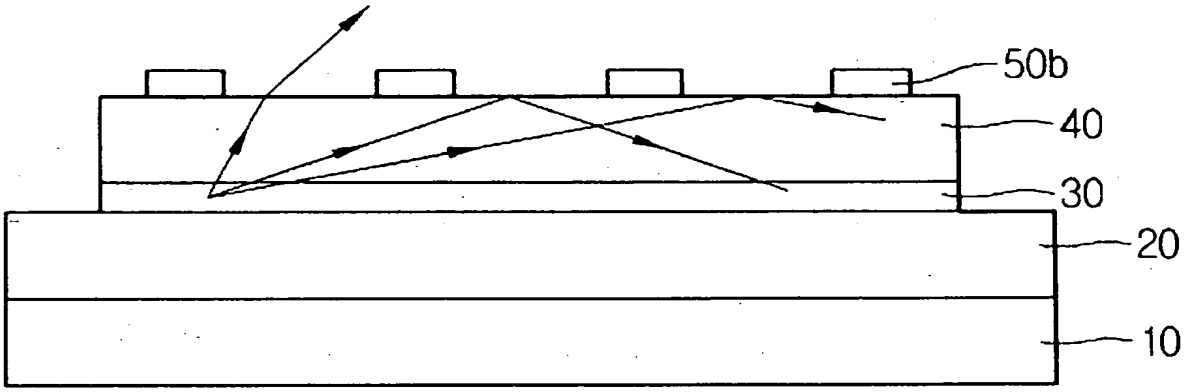
15. The light emitting diode as claimed in claim 13, wherein a temperature for the heat-treating is ranged from 90 ℃ to 400 ℃ .

16. The light emitting diode as claimed in claim 15, wherein the cylinder type prominence and depression element is formed by selectivity, said selectivity being partly changed due to a reaction of the metal and the semiconductor at time of etching.

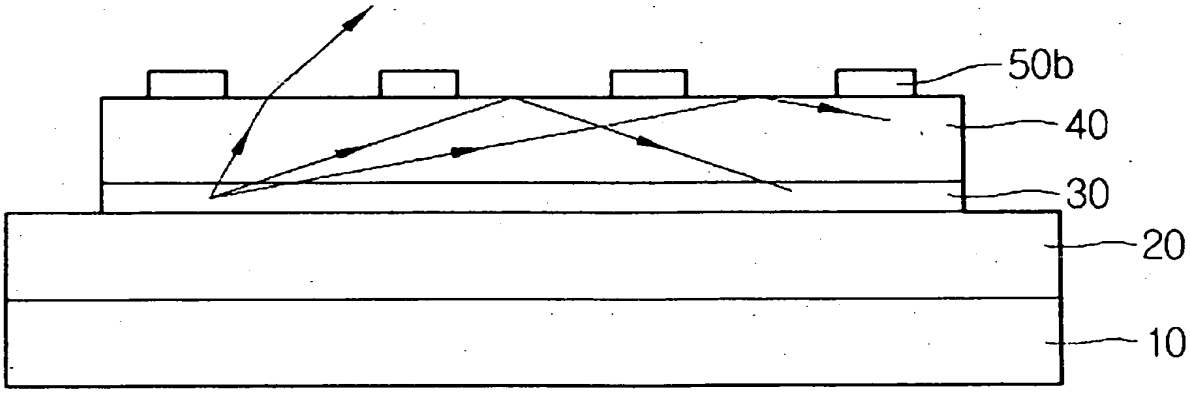
[Fig. 1]



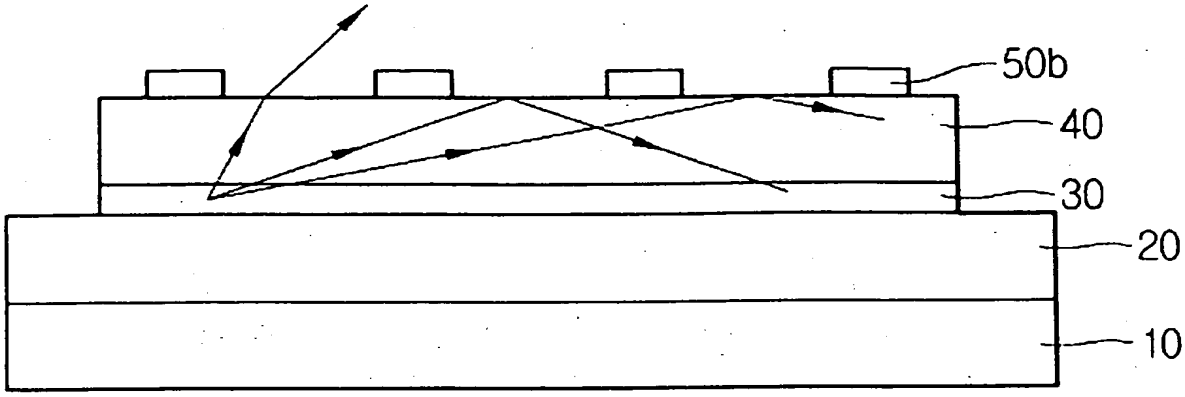
[Fig. 2]



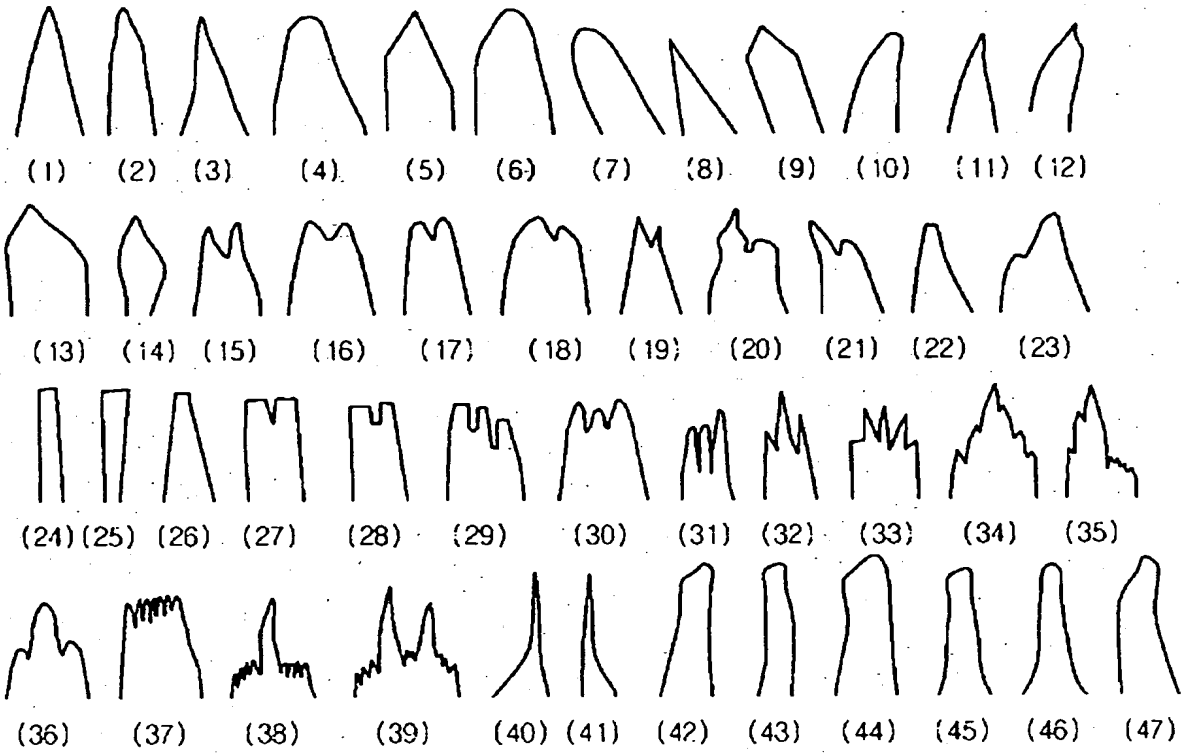
[Fig. 3]



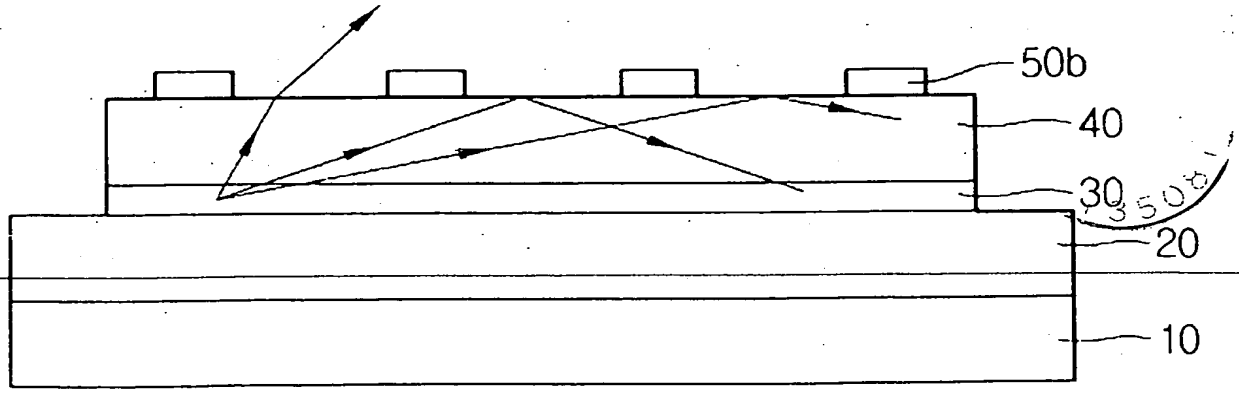
[Fig. 4]



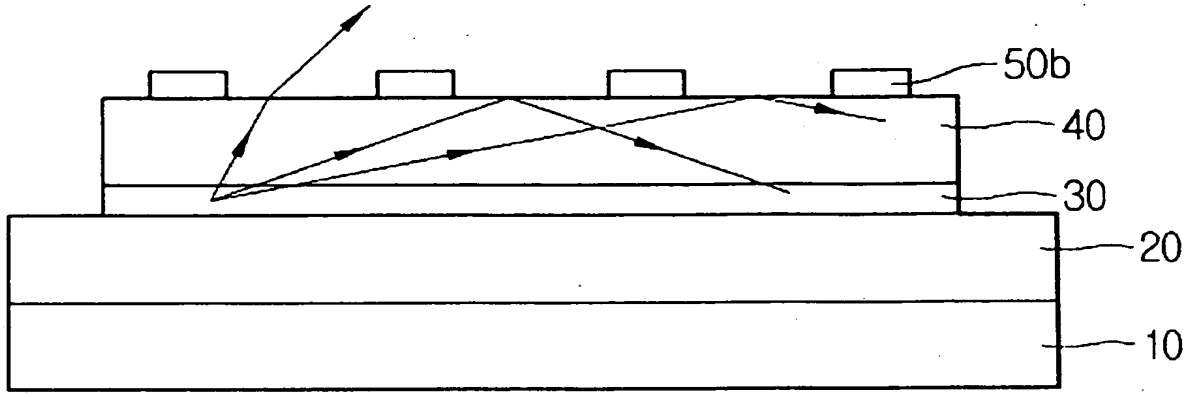
[Fig. 5]



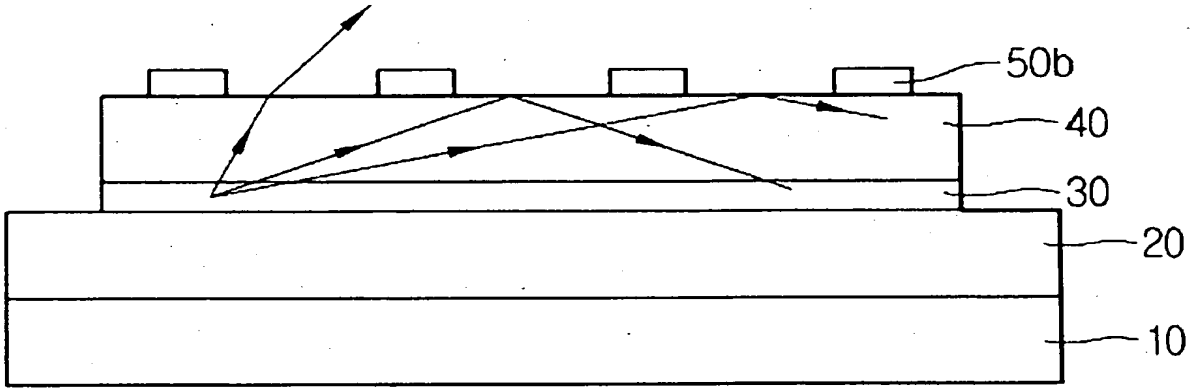
[Fig. 6]



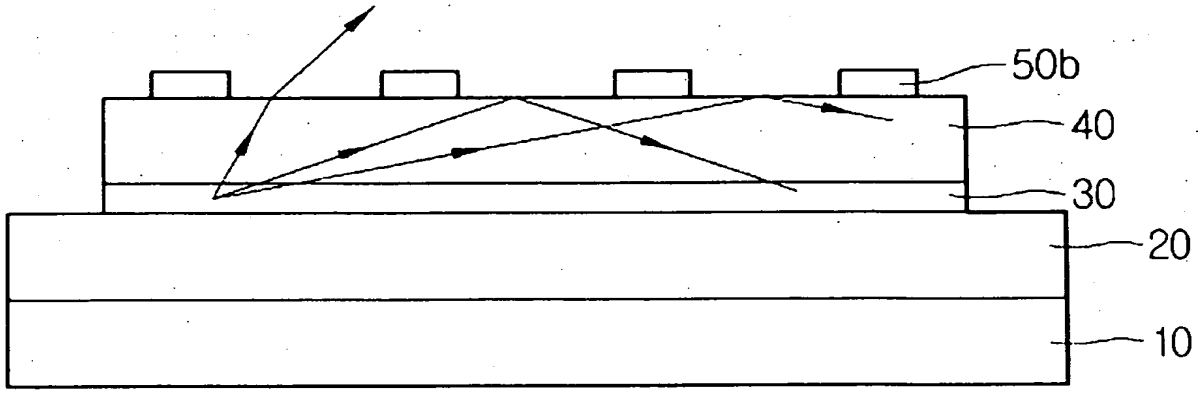
[Fig. 7]



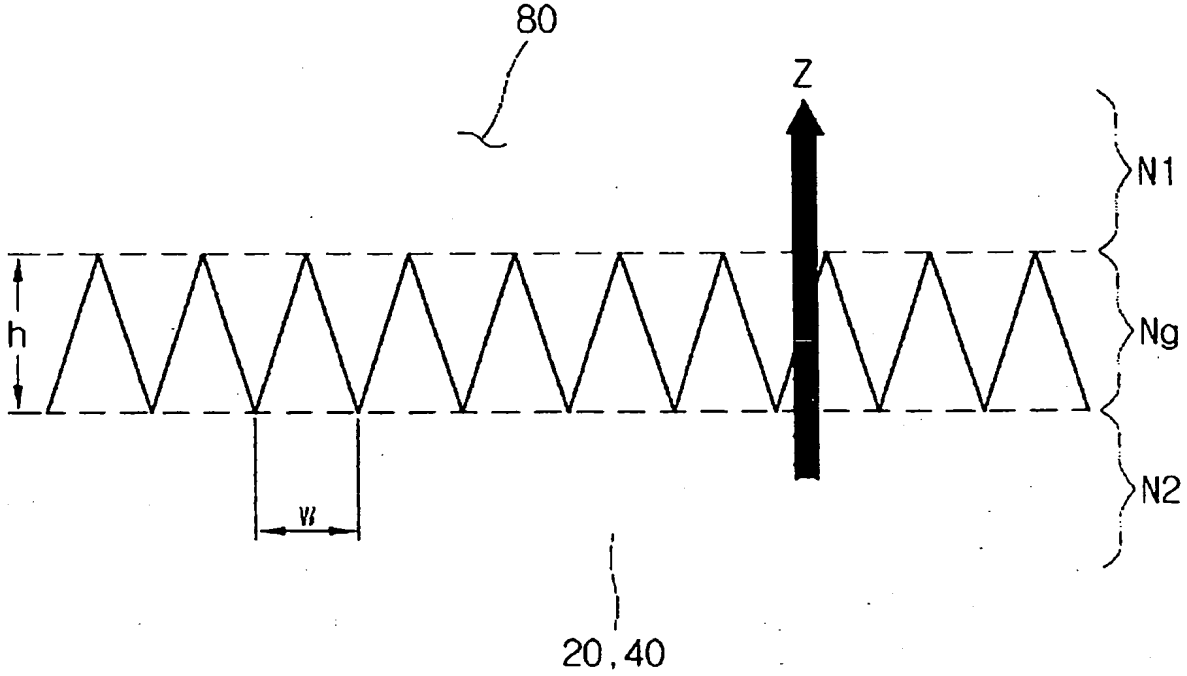
[Fig. 8]



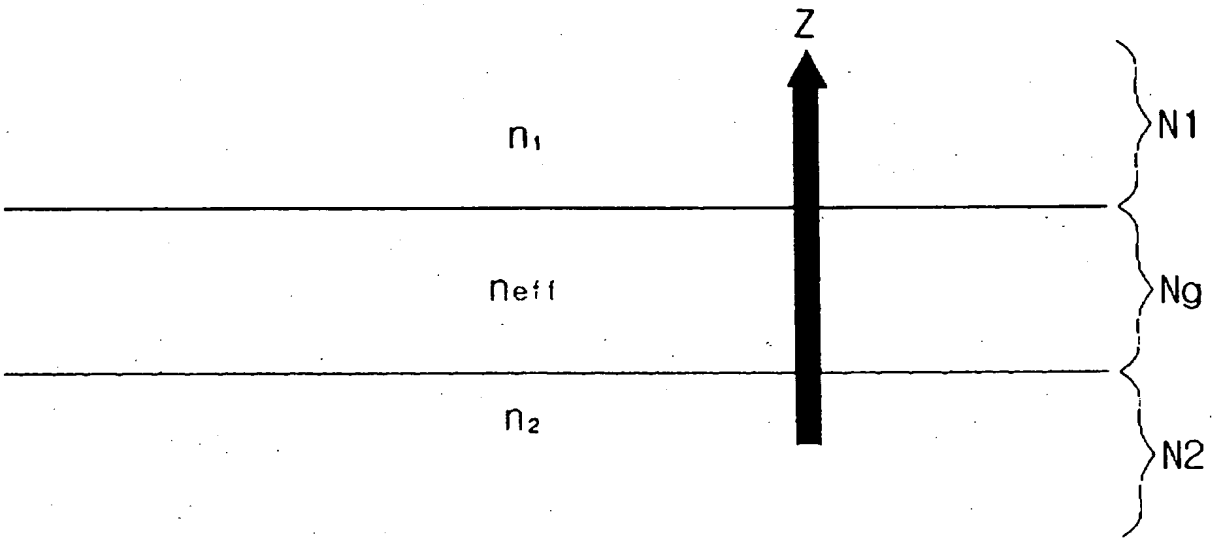
[Fig. 9]



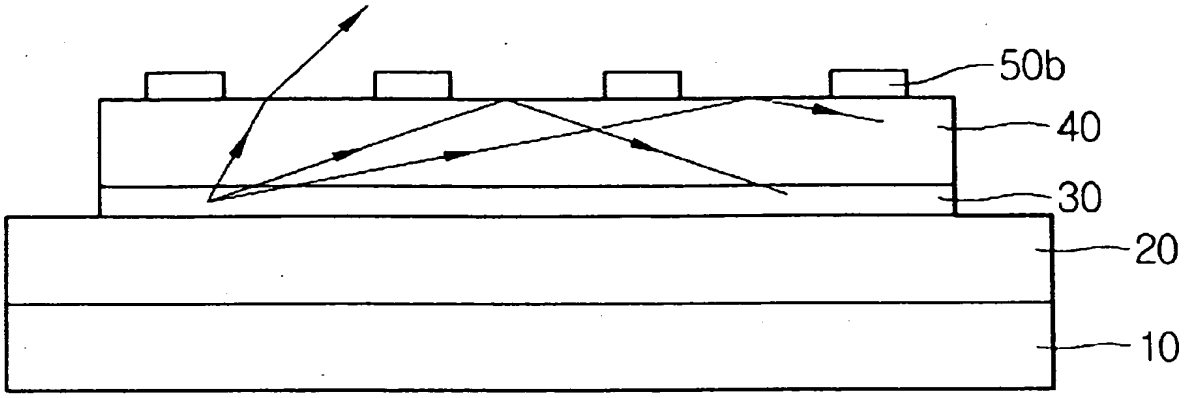
[Fig. 10]



[Fig. 11]



[Fig. 12]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2005/000036

A. CLASSIFICATION OF SUBJECT MATTER

IPC7 H01L 33/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L H01S

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean Patents and applications for inventions since 1975
Korean Utility models and applictions for Utility models since 1975
Japanese Utility models and application for Utility models since 1975

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
e-KIPASS ; "LED", "REFLECT", "ELECTRODE", "UNEVEN", "ROUGH"

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y A	US 6504180 B1 (IMEC VZW AND VRIJE UNIVERSITEIT) 7 JANUARY 2003 see the abstract, column 16 line 15 - line 37, figure 12	1-6 7-16
A	US 2003/0062530 A1 (KABUSHIKI KAISHA TOSHIBA) 3 APRIL 2003 see the abstract, paragraph [0087], claims 1-24, figures 1-9	1-16
E, Y E, A	KR 2005-0003671 A (EPIVALLEY CO., LTD.) 12 JANUARY 2005 see the abstract, figure 5	1-6 7-16

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"P" document published prior to the international filing date but later than the priority date claimed
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 APRIL 2005 (15.04.2005)	**15 APRIL 2005 (15.04.2005)**

Name and mailing address of the ISA/KR	Authorized officer
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Facsimile No. 82-42-472-7140	Telephone No. 82-42-481-5749

Form PCT/ISA/210 (second sheet) (January 2004)

INTERNATIONAL SEARCH REPORT

Information on patent family members

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